National Semiconductor

MM5307 Baud Rate Generator/Programmable Divider

General Description

The National Semiconductor MM5307 baud rate generator/programmable divider is a MOS/LSI P-channel enhancement mode device. A master clock for the device is generated either externally or by an on-chip crystal oscillator (Note 4). An internal ROM controls a divider circuit which produces the output frequency. Logic levels on the four control pins select between sixteen output frequencies. The frequencies are chosen from the following possible divisors: 2N, for $3 \leq N \leq 2048$; 2N + 1 and 2N + 0.5 for $4 \leq N \leq 2048$. Also one of the sixteen frequencies may be gated from the external frequency input. The MM5307AA is supplied with the divisors shown in the Control Table.

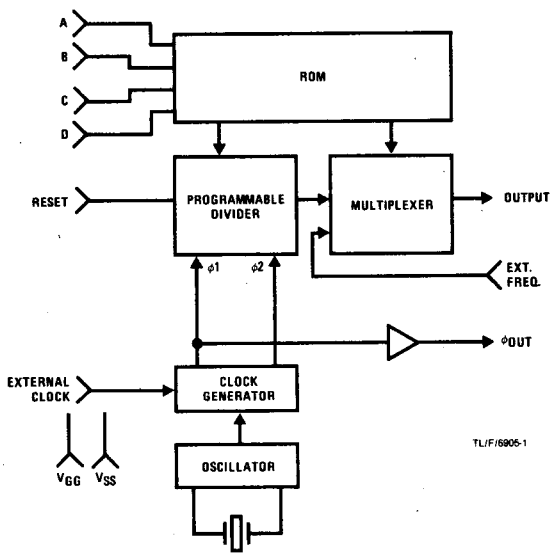
Features

- On-chip crystal oscillator
- Choice of 16 output frequencies from 1 crystal
- External frequency input pin
- Internal ROM allows generation of other frequencies on order
- Bipolar compatibility
- 0.01% accuracy (typ) exclusive of crystal
- 1 MHz master clock frequency

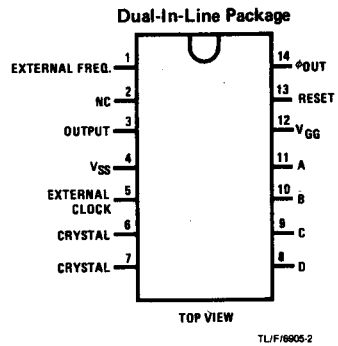
Applications

- UART clocks
- System clocks
- Electrically programmable counters

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number MM5307N
See NS Package N14A

Absolute Maximum Ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3V to V_{SS} − 20V	Operating Temperature	0°C to +70°C
Power Dissipation	700 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics

T_A within operating range, V_{SS} = 5V ±5%, V_{GG} = −12V ±5%, unless otherwise specified.

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	All Inputs (Except Crystal Pins)					
V_{IH}	Logical High Level		V_{SS}−1.5		V_{SS}+0.3	V
V_{IL}	Logical Low Level		V_{SS}−18		V_{SS}−4.2	V
	Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND			0.5	μA
	Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND, (Note 1)			7.0	pF
	External Clock Duty Cycle		40%		60%	
	Capacitance Measured Across Crystal Pins	f = 1 MHz, (Note 3)			5.0	pF
	Output Levels					
V_{OH}	Logical High Level	I_{SOURCE} = −0.5 mA	V_{SS}−2.6	V_{SS}		V
V_{OL}	Logical Low Level	I_{SINK} = 1.6 mA			V_{SS}−4.6	V
I_{GG}	Power Supply Current	f = 1 MHz			35	mA

AC Electrical Characteristics

T_A within operating range V_{SS} = 5V ±5%, V_{GG} = −12V ±5%, unless otherwise specified.

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Master Frequency		0.8		1.0	MHz
t_A	Access Time	C_L = 50 pF, (Note 2)			16	μs
t_{RD}	Reset Delay Time	f = Master Clock Frequency			500 + 4/f	ns
R_{PW}	Reset Pulse Width		500 + 4/f			ns
t_{OD}	Output Delay From Reset				500 + 4/f	ns
	Output Duty Cycle = 0.5T ± 1/f	T = Output Period f = Master Frequency	0.5T−1/f		0.5T+1/f	

Note 1: Capacitance is guaranteed by periodic measurement.

Note 2: Access time is defined as the time from a change in control inputs (A, B, C, D) to a stable output frequency. Access time is a function of frequency. The following formula may be used to calculate maximum access time for any master frequency: $T_A = 2.8\mu s + 1/f \times 13$, f is in MHz.

Note 3: The MM5307 is designed to operate with a 921.6 kHz parallel resonant crystal. When ordering the crystal a value of load capacitance (C_L) must be specified. This is the capacitance "seen" by the crystal when it is operating in the circuit. The value of C_L should match the capacitance measured at the crystal frequency across the crystal input pins on the MM5307. Any mismatch will be reflected as a very small error in the operating frequency. To achieve maximum accuracy, it may be necessary to add a small trimmer capacitor across the terminals.

Note 4: If the crystal oscillator is used Pin 5 (external clock) is connected to V_{SS}. If an external clock is used Pin 7 is connected to V_{SS}.

Control Table

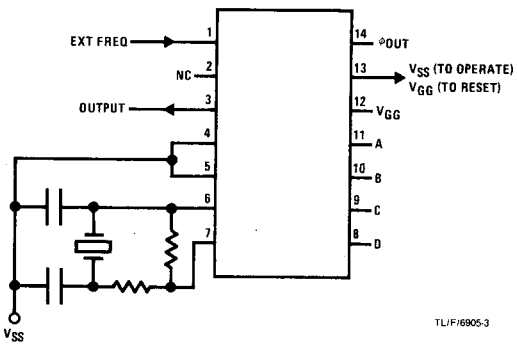
Input Freq: 921.6 kHz Master Clock

CONTROL PINS				NOMINAL BAUD RATES (OUTPUT FREQUENCY/16)			DIVISOR FOR AA
A	B	C	D	AA	AB	FAG	
0	0	0	1	50	50	50	1152
0	0	1	0	75	200	75	768
0	0	1	1	110	110	110	524
0	1	0	0	134.5	134.5	134.5	428.5
0	1	0	1	150	150	150	384
0	1	1	0	300	300	300	192
0	1	1	1	600	600	600	96
1	0	0	0	900	900	1050	64
1	0	0	1	1200	1200	1200	48
1	0	1	0	1800	1800	45.5	32
1	0	1	1	2400	2400	2400	24
1	1	0	0	3600	3600	56.9	16
1	1	0	1	4800	4800	4800	12
1	1	1	0	7200	75	66.7	8
1	1	1	1	9600	9600	9600	6
0	0	0	0	EXTERNAL FREQ			

Positive Logic: $1 = V_H$
$0 = V_L$

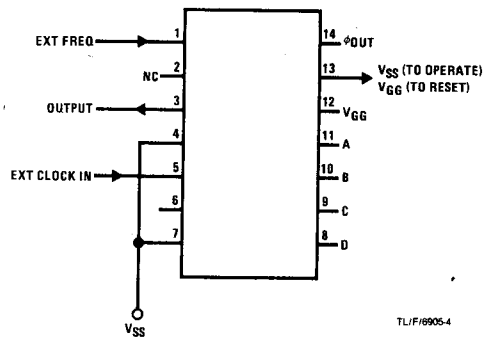
Typical Applications

Internal Oscillator



TL/F/6905-3

External Clock

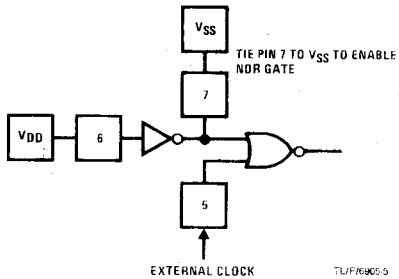


TL/F/6905-4

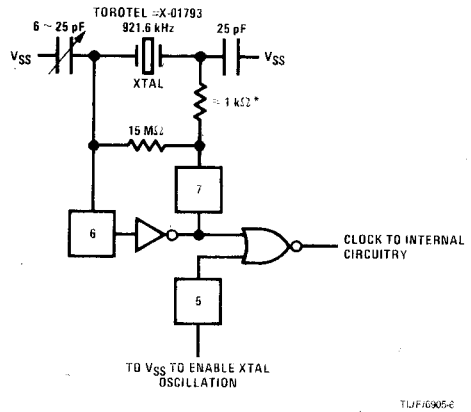
Application Hints

The external clock is brought in on pin 5 and pin 7 is tied to V_{SS} to enable the external clock input. Pin 6 can be left open; however, this may cause some current flow that can be eliminated by connecting pin 6 to V_{DD}.

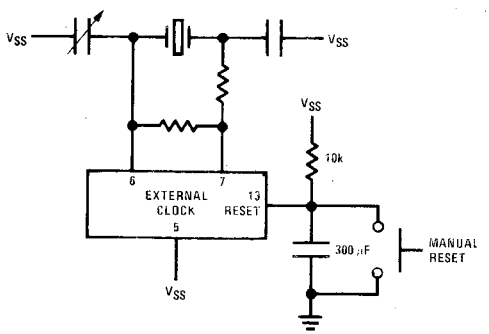
1) To use the MM5307 with an external clock, hook it up as follows:



2) To use a crystal directly:



*Component values should be selected based on crystal used.

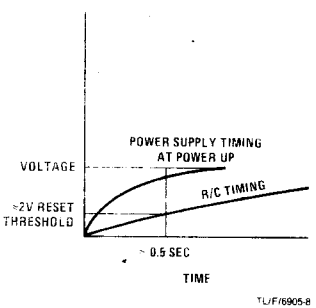


3) Reset (pin 13) must be at V_{SS} to operate. It may be necessary to take this to GND or V_{GG} to reset the ROM select circuit. An option is to tie ϕ out (pin 14) to external Freq In (pin 1), if not otherwise used.

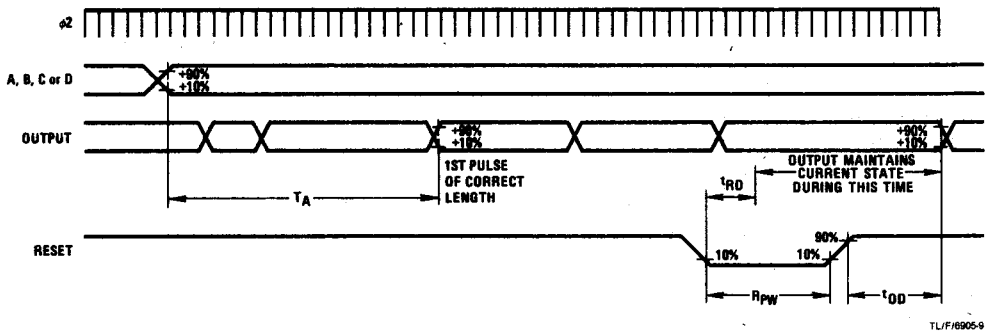
4) An interesting application might use two MM5307's in series to generate additional frequencies, i.e., with one programmed from the 921.6 kHz to 800 Hz out, a second could divide that by 16 to give a 50 Hz crystal controlled signal.

5) MM5307AA divisors are on the data sheet. AB divisors are the same as the AA except: 1) Code 0010 is divided by 288 → 32 kHz out, 200 baud; 2) Code 1110 is divided by 768 → 1.2 kHz, 75 baud.

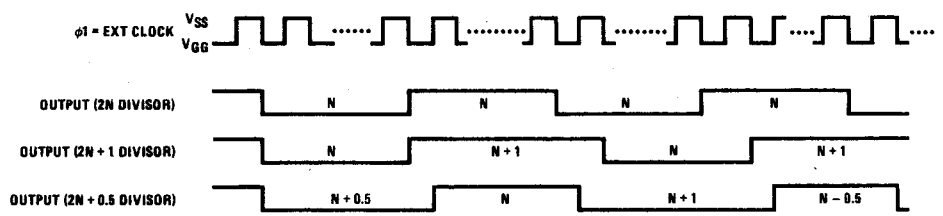
The MM5307 does not always generate an output when the power is up, even though the oscillator seems to be operating properly. In order to eliminate this problem, it is necessary to reset the chip at power "ON". This can be done manually, with a reset signal by a host system, or automatically by using R/C timing elements. The reset is done internally, when program inputs change. When using an R/C combination for auto resetting, the time constant must be several times larger than that of the power supply. For example, most lab power supplies take at least 0.5 sec for the voltage to reach 90% of full level. A 10 kΩ resistor and 300 µF capacitor combination should be adequate for most applications.



Timing Diagrams



TL/F/6905-9



TL/F/6905-10