HP 8160A
PROGRAMMABLE
PULSE GENERATOR

INCLUDING OPTIONS:
001, 020, 700, AND 907/8/9/10

SERVICE MANUAL
VOLUME 1

Serial Numbers

This manual applies to instruments with
serial numbers 2811G00796 and higher.

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INTRODUCTION

"Imagination is more important than knowledge."
Einstein

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1 PERFORMANCE TESTS

CONTENTS

INTRODUCTION

The performance tests verify the instruments specified performance characteristics.

They are suitable for incoming inspection, preventative maintainance, troubleshooting, and final test.

Make the Performance Tests in the order of occurance in the manual.

SAFETY

The HP 8160A is a Safety Class 1 instrument. It has an exposed metal chassis that is directly connected to earth potential through the line power cable.

Before testing the instrument review:

1. The Safety Summary, page ix (red page)
2. The Instrument Reference Manuals
3. The instrument safety markings.

TEST EQUIPMENT, RECOMMENDED

Recommended test equiment is listed in Appendix A.

ADJUSTMENT PROCEDURE NOTES

See the Adjustment Procedure Notes, Chapter 2, for additional test information

TEST RECORD

A test record is located at the end of this chapter. If a two channel instrument is tested, use two copies of the test record to record the test results, one for each channel.

The test results are identified as TR ENTRIES in the performance tests and on the test record.

1. PERIOD TEST

SPECIFICATIONS

Range:	20.0 ns to 999 ms.
Resolution:	3 digits, 0.1 ns minimum.
Accuracy:	PER < 100 ns = 3 % of programmed value ± 0.3 ns.
	PER => 100 ns = 2 % of programmed value.
Maximum Jitter:	0.1% of programmed value + 50 ps.
Repeatibility:	50 % of accuracy.

EQUIPMENT

1. Counter.
2. Cable, 50 ohm, BNC to BNC, coaxial.

SET-UP

1. Connect the HP 8160A's OUTPUT (A/B) to the counter's channel A input.
2. Set the HP 8160A: RCL 0.
3. Set the HP 8160A:
   a. INPUT MODE = NORM
   b. EXT SLOPE = POS
   c. PER = 20 ns
   d. DEL (A,B) = 0 ns
   e. WID (A,B) = 10 ns
   f. LEE (A,B) = 3 ns
   g. TRE (A,B) = 3 ns
   h. BUR = 0 BT
   i. HIL (A,B) = 1.0 V
   j. LOL (A,B) = -1.0 V
   k. OUTPUT MODE =A SEP B (OPTION 020)
      NORM (A,B)
      50 ohm (A,B)
      ENABLE
4. Set counter:
   a. FUNCTION = PERIOD A
   b. CHANNEL A = 50 ohm.

PROCEDURE

Check the HP 8160A period at the following PER settings:

	PER	ACCEPTABLE RANGE			TR ENTRY
1.*	20.0 ns	19.1 ns	-	20.9 ns	1-1
2.	99.9 ns	96.6 ns	-	103.2 ns	1-2
3.	100 ns	98.0 ns	-	102 ns	1-3
4.	999 ns	979.02 ns	-	1.02 us	1-4
5.	1.0 us	980 ns	-	1.02 us	1-5
6.	1.0 ms	980 us	-	1.02 ms	1-6
7.	999 ms	979.02 ms	-	1.02 s.	1-7

*Underprogramming to 18 ns is allowed to meet this specification.

2. BURST AND GATE TESTS

SPECIFICATIONS

Burst: 1 to 9999 pulses.
Gate: the gate signal synchronously turns the rate generator on and off. Thus, the first and last pulses are always completed.

EQUIPMENT

1. Counter
2. Pulse Generator
3. Cable, 50 ohm, BNC to BNC, coxial, 2 each.

SET-UP

1. Connect the HP 8160A's OUTPUT (A/B) to the counter's channel A input.
2. Connect the pulse generator's output to the HP 8160A's EXT INPUT.
3. Set the pulse generator.
   a. PER = 1 ms
   b. WID = 450 us
   c. DEL = 0 ns
   d. HIL = 1.0 V
   e. LOL = -1.0 V.
   f. MODE = TRIG
   g. EXT INPUT Slope = POS (positive).
4. Set counter.
   a. FUNCTION = START.
   b. CHANNEL A = 50 ohm
5. Set the HP 8160A: RCL 0

6. Set the HP 8160A.
   a. EXT SLOPE = POS
   b. PER = 100 us
   c. DEL (A,B) = 0 ns
   d. WID (A,B) = 50 ns
   e. LEE (A,B) = 3 ns
   f. TRE (A,B) = 3 ns
   g. BUR = 8160 BT
   h. HIL (A,B) = 1.0 V
   i. LOL (A,B) = -1.0 V
   j. OUTPUT MODE =A SEP B (OPTION 020)
      NORM (A,B)
      50 ohm (A,B)
      ENABLE

PROCEDURE

BURST TEST

1. Set the HP 8160A.
   a. INPUT MODE = BURST
   b. EXT SLOPE = POS (positive)
   c. EXT INPUT Impedance Switch = OFF
   d. TRIG LEVEL = middle position.

2. Reset the counter.

3. Press the HP 8160A's manual (MAN) button.
   NOTE: The HP 8160A is the instrument being tested.
4. Counter's reading = 8159*.
5. TR ENTRY = 2-1.

6. Set HP 8160A: EXT INPUT Impedance Switch = 50 ohm

7. Reset the counter

8. Press the pulse generator's manual (MAN) button.
   NOTE: The pulse generator is a piece of test equipment, not the HP 8160A being tested.
9. Counter's reading = 8159*.
10. TR ENTRY = 2-2.

GATE TEST

11. Set HP 8160A: INPUT MODE = GATE

12. Reset the counter
13. Press the pulse generator's manual (MAN) button.
    NOTE: The pulse generator is a piece of test equipment, not the HP 8160A being tested.
14. Counter reading = 4*.
15. TR ENTRY = 2-3.

*The readings are correct for the HP 5345A which uses the first pulse to arm the counting circuitry.

3. DELAY AND DOUBLE PULSE TESTS

There are four parts to the delay and double pulse tests.

1. Zero Delay Test
2. Minimum Delay Test
3. Double Pulse Test
4. Long Delay Test

NOTES: If the instrument has OPTION 020, repeat the entire delay and double test procedure for the second channel.

The specifications and tests are for minimum transistion times.

SPECIFICATIONS

DELAY

Range:	0.00 ns to 999 ms*
Resolution:	3 digits, 0.1 ns minimum
Accuracy:	1 % of programmed value ± 1 ns
Maximum Jitter:	0.1 % +50 ps (DEL <= 999ns)
	0.05 % (999 ns < DEL <= 9.99 us)
	0.005 % (DEL > 9.99 us)
Repeatiability:	50 % of accuracy.

DOUBLE PULSE

Range:	20.0 ns to 999 ms*
Resolution:	3 digits, 0.1 ns minimum
Accuracy:	1 % of programmed value ± 1 ns
Maximum Jitter:	0.1 % +50 ps (DBL <= 999 ns
	0.05 % (999 ns < DBL <= 9.99 us)
	0.005 % (DBL > 9.99 us)

*Duty Cycle Limits.
DELAY => 50 ns, DELAY maximum = 0.94 x PERIOD - 31 ns.
DELAY < 50 ns, DELAY maximum is independent of the PERIOD

EQUIPMENT

1. Pulse Generator
2. Sampling Scope, 50 ohm/20 dB TEE
3. Counter
4. Cables, 50 ohm, BNC to BNC, coaxial, 3 each.

SET-UP

1. Set pulse generator.
   a. PER = 100 ns
   b. WID = 50 ns
   c. HIL = 1.0 V LOL = 0.0 V

2. Set HP 8160A: RCL 0.

3. Set the HP 8160A.
   a. WID (A,B) = 8 ns
   b. DEL (A,B) = 0 ns
   c. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
   d. HIL (A,B) = 2.5 V LOL (A,B) = 0.0 V
   e. INPUT MODE = TRIG
   f. EXT INPUT = 50 ohm
   g. EXT SLOPE = POS (positive)

4. Connect the HP 8160A's TRIG OUTPUT via a 50 ohm/20 dB TEE to the scope's Channel A Input.
5. Connect the pulse generator's Output to the HP 8160A's EXT INPUT.
6. Connect the pulse generator's Trigger Output to the scope's Trigger Input
7. Adjust the HP 8160A TRIG LEVEL (trigger level).

PROCEDURE

PART 1 ZERO DELAY TEST

1. **SET REFERENCE:** Align the pulse's leading-edge 50%-point with the vertical center line of the scope's display.

2. Connect the HP 8160A's OUTPUT (A/B) via the 50 ohm/20 dB TEE to the scope's Channel A Input.
3. Measure the delay between the reference point and the pulse's leading-edge 50%-point.
4. LIMIT: <= ± 1 ns.
5. TR ENTRY = 3-1.

PART 2 MINIMUM DELAY TEST

SET-UP

1. Set the HP 8160A.
   a. PER (A,B) = 200 ns
   b. WID (A,B) = 8 ns
   c. DEL (A,B) = 0 ns
   d. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
   e. HIL (A,B) = 2.5 V LOL (A,B) = 0.0 V
   f. INPUT MODE = NORM

2. Connect the HP 8160A's OUTPUT (A/B) via a 50 ohm/20 dB TEE to the scope's Channel A input.
3. Connect the HP 8160A's TRIG OUTPUT to the scope's trigger input.

PROCEDURE

1. **SET REFERENCE:** Align the pulse's leading-edge 50%-point with the left line of the scope's display.

2. Check the HP 8160A delay at the following DEL settings:

DEL (A/B)		SPECIFIED LIMITS	TR ENTRY
a.	2 ns	2 ns ± 20 ps ± 1ns	3-2
b.	10 ns	10 ns ± 100 ps ± 1ns	3-3
c.	20 ns	20 ns ± 200 ps ± 1ns	3-4
d.	50 ns	50 ns ± 500 ps ± 1ns	3-5
e.	90 ns	90 ns ± 900 ps ± 1ns	3-6

PART 3 DOUBLE PULSE TEST

3. Check the HP 8160A double pulse delay at the following DBL settings:

DBL (A/B)		SPECIFIED LIMITS	TR ENTRY
a.*	20 ns	20 ns ± 200 ps ±1 ns	3-7
b.	80 ns	80 ns ± 800 ps ±1 ns	3-8

*Underprogramming to 18 ns is allowed to meet this specification.

PART 4 LONG DELAY TEST

EQUIPMENT

1. Counter
2. Cable, 50 ohm, BNC/BNC, coaxial, 2 each

SET-UP

1. Set the HP 8160A.
   a. PER (A,B) = 10 us
   b. WID (A,B) = 8 ns
   c. DEL (A,B) = 500 ns
   d. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
   e. HIL (A,B) = 2.5 V LOL (A,B) = 0.0 V

2. Set the counter.
   a. FUNCTION = TI A to B
   b. CHANNEL A = 50 ohm, POS (+) slope, DC, X1
   c. CHANNEL B = 50 ohm, POS (+) slope, DC, X1
   d. Gate Time = 10 ms
   e. INPUT MODE = SEP (SEPERATE)
   f. CHANNEL A/B trigger levels = 50% of pulse amplitudes

3. Connect the HP 8160A TRIG OUTPUT to the counter's Channel A input.
4. Connect the HP 8160A OUTPUT (A/B) to the counter's Channel B input.

PROCEDURE

1. Check the HP 8160A delay at the following PER and DEL settings:

	PER	DEL (A/B)	SPECIFIED LIMITS	TR ENTRY
a.	10 us	500 ns	500 ns ± 6 ns	3-9
b.	100 us	1.0 us	1.0 us ± 11 ns	3-10
c.	1.0 ms	50 us	50 us ± 0.5 us	3-11
d.	500 ms	1.0 ms	1.0 ms ± 10 us	3-12
e.	999 ms	500 ms	500 ms ± 5 ms	3-13
f.	999 ms	900 ms	900 ms ± 9 ms	3-14

4. WIDTH TEST

This test consists of two parts.

1. Minimum Width Test
2. Long Width Test

NOTES: If the instrument has OPTION 020, repeat the entire width test for the second channel.

The specifications and tests are for minimum transistion times.

SPECIFICATIONS

Range:	10.0 ns to 999 ms*
Resolution:	3 digits, 0.1 ns minimum
Accuracy:	1% of programmed value ± 1 ns
Maximum Jitter:	0.1% + 50 ps (WID <= 999 ns)
	0.05% (999 ns < WID <= 9.99 us)
	0.005% (WID > 9.99 us)
Repeatibility:	50% of accuracy.

*Duty Cycle Limits.
WIDTH => 50 ns, WIDTH maximum = 0.94 x PERIOD - 32 ns.
WIDTH < 50 ns, WIDTH maximum = 0.94 x PERIOD - 9 ns.

EQUIPMENT

1. Sampling scope, 50 ohm/20 dB TEE
2. Counter
3. Cables, 50 ohm BNC/BNC, coaxial, 2 each

PART 1 MINIMUM WIDTH TEST

SET-UP

1. Set the HP 8160A: RCL 0.
2. Set the HP 8160A.
   a. PER = 200 ns
   b. WID (A,B) = 10 ns
   c. DEL (A,B) = 0 ns
   d. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
   e. HIL (A,B) = +2.0 V LOL (A,B) = -2.0 V
3. Connect the HP 8160A's OUTPUT (A/B) via a 50 ohm/20 dB TEE to the scope's Channel A input.
4. Connect the HP 8160A's TRIG OUTPUT to the scope's trigger input.

PROCEDURE

1. **SET REFERENCE:** Align the pulse's leading-edge 50%-point with the left line of the scope's display.
2. Check the HP 8160A pulse width at the following WID settings:

	WIDTH (A/B)	SPECIFIED LIMITS	TR ENTRY
a.*	10 ns	10 ns ± 1.1 ns	4-1
b.	50 ns	50 ns ± 1.5 ns	4-2
c.	80 ns	80 ns ± 1.8 ns	4-3

*Underprogramming to 8 ns is allowed to meet this specification.

PART 2 LONG WIDTH TESTS

SET-UP

1. Set the HP 8160A.
   a. PER = 1 ms
   b. WID (A,B) = 500 ns
   c. DEL (A,B) = 0 ns
   d. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
   e. HIL (A,B) = +2.0 V LOL (A,B) = -2.0 V

2. Set the counter.
   a. FUNCTION = TI A to B
   b. Channel A = 50 ohm, POS (+) slope, X1, DC
   c. Channel B = 50 ohm, NEG (-) slope, X1, DC
   d. GATE TIME = as necessary
   e. Channel A/B Trigger Levels = PRESET
   f. INPUT MODE = COM (COMMON)

PROCEDURE

1. Check the HP 8160A pulse width at the following PER and WID settings:

	PER	WID (A/B)	SPECIFIED LIMIT	TR ENTRY
a.	1 ms	500 ns	500 ns ± 6 ns	4-4
b.	1 ms	1 us	1 us ± 11 ns	4-5
c.	1 ms	50 us	50 us ± 0.5 us	4-6
d.	500 ms	1 ms	1 ms ± 10 us	4-7
e.	999 ms	500 ms	500 ms ± 5 ms	4-8
f.	999 ms	900 ms	900 ms ± 9 ms.	4-9

5. FAST TRANSITION TIME TEST

If OPTION 020 is installed, repeat the fast transition time test for the second channel.

SPECIFICATIONS

NOTE: These specifications and tests apply to 50 ohm sources and 50 ohm loads.

Range:	6 ns to 9.99 ms
Resolution:	3 digits, 100 ps minimum
Accuracy:	3% of programmed value ± 1 ns
Repeatability:	50% of accuracy
Linearity:	3% for transisition times => 30 ns

EQUIPMENT

1. Sampling scope, 50 ohm/20 dB TEE
2. Cables, 50 ohm, BNC/BNC, coaxial, two each

SET-UP

1. Set the HP 8160A: RCL 0.
2. Set the HP 8160A.
   a. PER = 100 ns
   b. WID (A,B) = 50 ns
   c. DEL (A,B) = 0 ns
   d. LEE (A,B) = 6 ns TRE (A,B) = 6 ns.
3. Set the scope.
   a. Horizontal sensitivity = 1 ns/division.
   b. Vertical sensitivity = 1 V/division.
   c. OUTPUT MODE = NORM (NORMAL).
4. Connect the HP 8160A's OUTPUT via a 50 ohm/20 dB TEE to the scope's Channel A input.
5. Connect the HP 8160A TRIG OUTPUT to the scope's trigger input.

PROCEDURE

1. Set HP 8160A: HIL (A/B) = 8.0 V LOL (A/B) = 0.0 V

2. Measure the pulse rise-time from the 10% to the 90% points.
3. LIMIT* = 6 ns ± 1.18 ns.
4. TR ENTRY = 5-1.

5. Measure the pulse fall-time from the 90% to the 10% points.
6. LIMIT *= 6 ns ± 1.18 ns.
7. TR ENTRY = 5-2.

8. Set HP 8160A: LEE (A/B) = 20 ns, TRE (A/B) = 20 ns.
9. Measure the rise- and fall-times.
10. LIMIT = 20 ns ± 1.6 ns.
11. TR ENTRY = 5-3 and 5-4.

12. Set HP 8160A: LEE (A/B) = 30 ns, TRE (A/B) = 30 ns.
13. Measure the rise- and fall-times.
14. LIMIT = 30 ns ± 1.9 ns.
15. TR ENTRY = 5-5 and 5-6.

*Underprogramming to 3 ns is allowed to meet this specification.

6. SLOW TRANSITION TIME TEST

If OPTION 020 is installed, repeat the slow transition time test for the second channel.

NOTE: This test requires the HIL = 9.99 V voltage level measured in the High Level Test. It is used to set the time interval probes.

SPECIFICATIONS

The specifications are listed in Chapter 4-10.4.

EQUIPMENT

1. Counter
2. Time Interval Probes and Time Interval Probe Adapter
3. Cable, 50 ohm, BNC/BNC, coaxial, three each.

SET-UP

1. Set the HP 8160A: RCL 0.
2. Set the HP 8160A.
   a. PER = 10 us
   b. WID (A,B) = 500 ns
   c. DEL (A,B) = 0 ns
   d. LEE (A,B) = 200 ns TRE (A,B) = 200 ns
   e. HIL (A,B) = 9.99 V LOL (A,B) = 0 V.

3. Set the time interval probes.
   a. Start channel = 'A +XX.X POSITIVE SLOPE'
   b. Stop channel = 'A +YY.Y POSITIVE SLOPE'
   NOTE: XX.X and YY.Y are values calculated from the measured value of HIL = 9.99 V in Test 7.
   XX.X = the pulse's 10% point.
   YY.Y = the pulse's 90% point.

4. Set the counter.
   a. FUNCTION = TI A to B (time interval)
   b. INPUT MODE = SEP (SEPERATE)
   c. Channel A = 50 ohm, X1, + slope, AC
   d. Channel B = 50 ohm, X1, + slope, AC
   e. Channel A/B Trigger Levels = Preset

5. Connect the Time Interval Channel A probe to a TI probe adapter.
6. Attach a 50 termination to the TI probe adapter.
7. Attach a BNC cable to the TI probe adapter.

8. Connect the TI Probe's rear panel outputs to the counter inputs.
   a. START output to Channel A input.
   b. STOP output to Channel B input.

9. **CALIBRATE** the time interval probes.
   Perform the LEVEL operation; hold the CAL switch in the LEVEL position until the channel leds are on.

   NOTE: Perform the calibration with the TEE, 50 ohm termination, and the cable attached.

10. Conncect the BNC cable from the TI probe adapter to the HP 8160A's OUTPUT (A/B).

PROCEDURE

1. Check the HP 8160A OUTPUT (A/B) rise-times at the following PERIOD, WIDTH (A/B), LEADING EDGE (A/B), and TRAILING EDGE (A/B) settings:

	SETTING	SPECIFIED LIMITS	TR ENTRY
a.	PER = 10 us WID = 500 ns LEE = 200 ns TRE = 200 ns	200 ns ± 7 ns	6-1
b.	PER = 1 ms WID = 500 us LEE = 1 us TRE = 1 us	1 us ± 31 ns	6-2
c.	PER = 1 ms WID = 500 us LEE = 100 us TRE = 100 us	100 us ± 3 us	6-3
d.	PER = 10 ms WID = 5 ms LEE = 1 ms TRE = 1 ms	1 ms ± 30 ms	6-4
e.	PER = 100 ms WID = 50 ms LEE = 9.9 ms TRE = 9.9 ms	9.9 ms ± 0.3 ms.	6-5

2. Set the time interval probes.
   a. START channel = 'A +YY.Y NEGATIVE SLOPE'
   b. STOP channel = 'A +XX.X NEGATIVE SLOPE'

3. Check the HP 8160A (OUTPUT A/B) fall-times at the following PERIOD, WIDTH (A/B), LEADING EDGE (A/B), and TRAILING EDGE (A/B) settings:

	SETTING	SPECIFIED LIMITS	TR ENTRY
a.	PER = 10 us WID = 500 ns LEE = 200 ns TRE = 200 ns	200 ns ± 7 ns	6-6
b.	PER = 1 ms WID = 500 us LEE = 1 us TRE = 1 us	1 us ± 31 ns	6-7
c.	PER = 1 ms WID = 500 us LEE = 100 us TRE = 100 us	100 us ± 3 us	6-8
d.	PER = 10 ms WID = 5 ms LEE = 1 ms TRE = 1 ms	1 ms ± 30 ms	6-9
e.	PER = 100 ms WID = 50 ms LEE = 9.9 ms TRE = 9.9 ms	9.9 ms ± 0.3 ms.	6-10

7. HIGH LEVEL (HIL) AND LOW LEVEL (LOL) TESTS

If OPTION 020 is installed, repeat the high level and low level tests for the second channel.

SPECIFICATIONS

NOTE: This specification applies to 50 ohm sources and 50 ohm loads.

High Level range:	-9.89 V to 9.99 V.
Low Level range:	-9.99 V to 9.89 V.
Resolution:	3 digits, 10.0 mV.
Level Accuracy:	1% of programmed value ± 1% of pulse amplitude, ± 50 mV pulse shift.
Repeatability:	50% of the specified value.
Settling time:	40 ns to specified accuracy.
Minimum amplitude:	0.1 V.
Maximum amplitude:	9.99 V

EQUIPMENT

1. Multimeter
2. 50 ohm feedthrough termination, **0.1%, 10 W**
3. Adapter, BNC to dual banana plug
4. Cables, BNC to BNC, two each.

SET-UP

1. Set the HP 8160A: RCL 0
2. Set the HP 8160A.
   a. PER = 100 ms
   b. WID (A/B) = 50 ms
   c. LEE (A/B) = 3 ns TRE (A/B) = 3 ns
   d. OUTPUT MODE =NORM (A/B)
      ENABLE
3. Set the Multimeter (HP 3478).
   a. SGL TRIG = Single Trigger
   b. Blue/AUTO ZERO = Auto Zero off
   c. BLUE/4 = 4 digits
4. Connect the HP 8160A OUTPUT (A/B) to the Multimeter's input via a 50 ohm feedthrough (0.1%, **10 W**) and a BNC to dual banana plug adapter.
5. Connect the HP 8160A TRIG OUTPUT to the Multimeter's trigger input.

PROCEDURE

HIGH LEVEL TEST

1. Set the HP 8160A.

   a. DEL (A/B) = 80 ms
   b. LOL (A/B) = 0.0 V
   c. OUTPUT (A/B) = 50 ohm
   d. OUTPUT MODE =NORM (A/B)
      ENABLE

2. Check the HP 8160A OUTPUT (A/B) high levels at the following HIL settings:

	HIL (A/B)	SPECIFIED LIMITS	TR ENTRY
a.	0.10 V	100 mV ± 52 mV	7-1
b.	0.49 V	490 mV ± 60 mV	7-2
c.	0.99 V	990 mV ± 70 mV	7-3
d.	1.99 V	1.99 V ± 90 mV	7-4
e.	2.99 V	2.99 V ± 110 mV	7-5
f.	3.99 V	3.99 V ± 130 mV	7-6
g.	7.99 V	7.99 V ± 210 mV	7-7
h.	9.99 V	9.99 V ± 250 mv	7-8

3. Set the HP 8160A: OUTPUT MODE = 1 k ohm (A/B).

4. Check the HP 8160A OUTPUT (A/B) high levels at the following HIGH LEVEL (HIL) settings:

	HIL (A/B)	SPECIFIED LIMITS	TR ENTRY
a.	10.0 V	10.0 V ± 300 mV	7-9
b.	13.0 V	13.0 V ± 360 mV	7-10
c.	17.0 V	17.0 V ± 440 mV	7-11
d.	19.9 V	19.9 V ± 500 mV	7-12

LOW LEVEL TEST

1. Set the HP 8160A.
   a. DEL (A/B) = 30 ms
   b. HIL (A/B) = -0.0 V
   c. OUTPUT (A/B) = 50 ohm

2. Check the HP 8160A OUTPUT (A/B) low levels at the following LOL settings:

LOL (A/B)	SPECIFIED LIMITS	TR ENTRY
a. -0.10 V	-100m V ± 52 mV	7-13
b. -0.49 V	-490m V ± 60 mV	7-14
c. -0.99 V	-990m V ± 70 mV	7-15
d. -1.99 V	-1.99 V ± 90 mV	7-16
e. -2.99 V	-2.99 V ± 110 mV	7-17
f. -3.99 V	-3.99 V ± 130 mV	7-18
g. -7.99 V	-7.99 V ± 210 mV	7-19
h. -9.99 V	-9.99 V ± 250 mv	7-20

3. Set the HP 8160A: OUTPUT MODE = 1 k ohm (A/B).

4. Check the HP 8160A OUTPUT (A/B) low levels at the following LOW LEVEL (LOL) settings:

LOL (A/B)	SPECIFIED LIMITS	TR ENTRY
a. -10.0 V	-10.0 V ± 300 mV	7-21
b. -13.0 V	-13.0 V ± 360 mV	7-22
c. -17.0 V	-17.0 V ± 440 mV	7-23
d. -19.9 V	-19.9 V ± 500 mV	7-24

8. A ADD B AMPLITUDE TEST

SPECIFICATIONS

NOTES: OPTION 020 INSTRUMENTS ONLY

These specifications apply only to 50 ohm loads and 50 ohm sources.

Level Accuracy:	reduced by <= 2.5%.
Amplitude Range:	200 mV to 19.9 V

EQUIPMENT

1. Multimeter
2. BNC to dual banana plug adapter
3. Cables, BNC, two each.

SET-UP

1. Set the HP 8160A.
   a. RCL 0.
   b. OUTPUT MODE = A ADD B.

2. Set the HP 8160A.
   a. PER = 100 ms
   b. WID (A,B) 50 ms
   c. DEL (A,B) = 80 ms
   d. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
   e. HIL (A,B0 = 2.5 V LOL (A,B) = -2.5 V.

3. Set Multimeter (HP 3478).
   a. SGL TRG = Single Trigger
   b. Blue/AUTO ZERO = AUTO ZERO off
   c. Blue/4 = 4 digits

4. Connect the HP 8160A's OUTPUT to the Multimeter's input via a 50 ohm feedthrough **(0.1%, 10 W)** and a BNC to dual banana plug adapter.
5. Connect the HP 8160A TRIG OUTPUT to the Multimeter's trigger input.

PROCEDURE

HIGH LEVEL TEST

1. Set the HP 8160A: DEL (A,B) = 80 ms.

2. Check the HP 8160A added high levels at the following HIL and LOL settings:

	HIL (A,B)	LO (A,B)	SPECIFIED LIMITS	TR ENTRY
a.	2.50 V	-2.50 V	5.00 V + 0 V/-125 mV	8-1
b.	3.75 V	-3.75 V	7.50 V + 0 V/-188 mV	8-2
c.	4.99 V	-4.99 V	9.98 V + 0 V/-250 mV.	8-3

LOW LEVEL TEST

1. Set the HP 8160A: DEL (A,B) = 30 ms.

2. Check the HP 8160A added low levels at the following HIL and LOL settings:

	HIL (A,B)	LOL (A,B)	SPECIFIED LIMITS	TR ENTRY
a.	2.50 V	-2.50 V	-5.00 V + 0 V/-125 mV	8-4
b.	3.75 V	-3.75 V	-7.50 V + 0 V/-188 mV	8-5
c.	4.99 V	-4.99 V	-9.98 V + 0 V/-250 mV.	8-6

9. PULSE ABERRATION TEST

If OPTION 020 is installed, repeat this test for the second channel.

SPECIFICATIONS

Preshoot, overshoot, and ringing, must be
<= 5% of the pulse amplitude ± 10 mV.

EQUIPMENT

1. Sampling scope, 50 ohm/20dB TEE
2. Cable, BNC, two each.

SET-UP

1. Set the HP 8160A: RCL 0.
2. Set the HP 8160A.
   a. PER = 100 ns
   b. WID (A/B) = 50 ns
   c. DEL (A/B) = 0 ns
   d. HIL (A/B) = 8.0 V LOL (A/B) = 0.0 V
   e. LEE (A/B) = 6 ns TRE (A/B) = 6 ns

3. Set the scope.
   a. Horizontal Amplifier = NORM, 1 ns/division.
   b. Vertical Amplifier
      1.) Center trace on lowest graticule.
      2.) Set for 1 V/division.

4. Connect the HP 8160A's OUTPUT (A/B) to the scope's Channel A input.
5. Connect the HP 8160A's TRIG OUTPUT to the scope's trigger input.

PROCEDURE

Check the following HP 8160A OUTPUT (A/B) pulse characteristics:

	CHARACTERISTIC	SPECIFIED LIMIT	TR ENTRY
1.	Preshoot	*	9-1
2.	Overshoot	*	9-2
3.	Ringing	*	9-3

* <= 5% of the pulse amplituce ± 10 mV.

PERFORMANCE TEST RECORD

MODEL: HP 8160A TESTED BY:_____

SERIAL NUMBER:_____ DATE:_____

COMMENTS:_____

TEST	LIMIT MINIMUM	ACTUAL (TR ENTRY)	LIMIT MAXIMUM	PASS	FAIL
PERIOD:					
20 ns	19.1 ns	(1-1)_____	20.9 ns	_____	_____
99.9 ns	96.6 ns	(1-2)_____	103.2 ns	_____	_____
100 ns	98.0 ns	(1-3)_____	102 ns	_____	_____
999 ns	979.02 ns	(1-4)_____	1.02 us	_____	_____
1 us	980 ns	(1-5)_____	1.02 us	_____	_____
1 ms	980 us	(1-6)_____	1.02 ms	_____	_____
999 ms	979.02 ms	(1-7)_____	1.02 s.	_____	_____
BURST:					
8160		(2-1)_____		_____	_____
8160		(2-2)_____		_____	_____
GATE:					
5		(2-3)_____		_____	_____
ZERO DELAY:					
0 ns	-1.0 ns	(3-1)_____	+1.0 ns	_____	_____

TEST	LIMIT MINIMUM	ACTUAL (TR ENTRY)	LIMIT MAXIMUM	PASS	FAIL
MINIMUM DELAY:					
2 ns	980 ps	(3-2)_____	3.02 ns	_____	_____
10 ns	8.90 ns	(3-3)_____	11.1 ns	_____	_____
20 ns	18.8 ns	(3-4)_____	21.2 ns	_____	_____
50 ns	48.5 ns	(3-5)_____	51.5 ns	_____	_____
90 ns	88.1 ns	(3-6)_____	91.9 ns	_____	_____
DOUBLE PULSE:					
20 ns	18.8 ns	(3-7)_____	21.2 ns	_____	_____
80 ns	78.2 ns	(3-8)_____	81.8 ns	_____	_____
LONG DELAY:					
500 ns	494 ns	(3-9)_____	506 ns	_____	_____
1 us	990 ns	(3-10)_____	1.01 us	_____	_____
50 us	49.5 us	(3-11)_____	50.5 us	_____	_____
1 ms	990 us	(3-12)_____	1.01 us	_____	_____
500 ms	495 ms	(3-13)_____	505 ms	_____	_____
900 ms	891 ms	(3-14)_____	909 ms	_____	_____
MINIMUM WIDTH:					
10 ns	8.9 ns	(4-1)_____	11.1 ns	_____	_____
50 ns	48.5 ns	(4-2)_____	51.5 ns	_____	_____
80 ns	78.2 ns	(4-3)_____	81.8 ns	_____	_____
LONG WIDTH:					
500 ns	494 ns	(4-4)_____	506 ns	_____	_____
1 us	990 ns	(4-5)_____	1.01 us	_____	_____
50 us	49.5 us	(4-6)_____	50.5 us	_____	_____
1 ms	990 us	(4-7)_____	1.01 ms	_____	_____
500 ms	495 ms	(4-8)_____	505 ms	_____	_____
900 ms	891 ms	(4-9)_____	909 ms	_____	_____

TEST	LIMIT MINIMUM	ACTUAL (TR ENTRY)	LIMIT MAXIMUM	PASS	FAIL
FAST TRANSITION:					
6 ns	4.82 ns	(5-1)_____	7.18 ns	_____	_____
6 ns	4.82 ns	(5-2)_____	7.18 ns	_____	_____
20 ns	18.4 ns	(5-3)_____	21.6 ns	_____	_____
20 ns	18.4 ns	(5-4)_____	21.6 ns	_____	_____
30 ns	28.1 ns	(5-5)_____	31.9 ns	_____	_____
30 ns	28.1 ns	(5-6)_____	31.9 ns	_____	_____
SLOW TRANSITION:					
200 ns	193 ns	(6-1)_____	207 ns	_____	_____
1 us	969 ns	(6-2)_____	1.031 us	_____	_____
100 us	97 us	(6-3)_____	103 us	_____	_____
1 ms	970 us	(6-4)_____	1.030 ms	_____	_____
9.9 ms	9.6 ms	(6-5)_____	10.2 ms	_____	_____
200 ns	193 ns	(6-6)_____	207 ns	_____	_____
1 us	969 ns	(6-7)_____	1.031 us	_____	_____
100 us	97 us	(6-8)_____	103 us	_____	_____
1 ms	970 us	(6-9)_____	1.030 ms	_____	_____
9.9 ms	9.6 ms	(6-10)_____	10.2 ms	_____	_____

TEST	LIMIT MINIMUM	ACTUAL (TR ENTRY)	LIMIT MAXIMUM	PASS	FAIL
HIGH LEVEL:					
0.10 V	48 mV	(7-1)_____	152 mV	_____	_____
0.49 V	430 mV	(7-2)_____	550 mV	_____	_____
0.99 V	920 mV	(7-3)_____	1.06 V	_____	_____
1.99 V	1.9 V	(7-4)_____	2.08 V	_____	_____
2.99 V	2.88 V	(7-5)_____	3.01 V	_____	_____
3.99 V	3.86 V	(7-6)_____	4.02 V	_____	_____
7.99 V	7.78 V	(7-7)_____	8.00 V	_____	_____
9.99 V	9.74 V	(7-8)_____	10.24 V	_____	_____
10.0 V	9.7 V	(7-9)_____	10.3 V	_____	_____
13.0 V	12.64 V	(7-10)_____	13.36 V	_____	_____
17.0 V	16.56 V	(7-11)_____	17.44 V	_____	_____
19.9 V	19.4 V	(7-12)_____	20.4 V	_____	_____
LOW LEVEL:					
-0.10 V	-152 mV	(7-13)_____	-48 mV	_____	_____
-0.49 V	-550 mV	(7-14)_____	-430 mV	_____	_____
-0.99 V	-1.06 V	(7-15)_____	920 mV	_____	_____
-1.99 V	-1.08 V	(7-16)_____	-1.9 V	_____	_____
-2.99 V	3.1 V	(7-17)_____	-2.88 V	_____	_____
-3.99 V	-4.12 V	(7-18)_____	-3.86 V	_____	_____
-7.99 V	-8.2 V	(7-19)_____	-7.78 V	_____	_____
-9.99 V	10.24 V	(7-20)_____	-9.74 V	_____	_____
-10.0 V	-10.3 V	(7-21)_____	-9.7 V	_____	_____
-13.0 V	-13.36 V	(7-22)_____	-12.64 V	_____	_____
-17.0 V	-17.44 V	(7-23)_____	-16.56 V	_____	_____
-19.9 V	-20.4 V	(7-24)_____	-19.4 V	_____	_____

TEST	LIMIT MINIMUM	ACTUAL (TR ENTRY)	LIMIT MAXIMUM	PASS	FAIL
A ADD B:					
5.00 V	4.875 V	(8-1)_____	5.00 V	_____	_____
7.50 V	7.312 V	(8-2)_____	7.50 V	_____	_____
9.98 V	9.730 V	(8-3)_____	9.98 V	_____	_____
-5.00 V	-5.125 V	(8-4)_____	-5.00 V	_____	_____
-7.50 V	-7.688 V	(8-5)_____	-7.50 V	_____	_____
-9.98 V	-10.230 V	(8-6)_____	-9.98 V	_____	_____
PULSE ABERRATION:					
Preshoot *		(9-1)_____		_____	_____
Overshoot *		(9-2)_____		_____	_____
Ringing *		(9-3)_____		_____	_____

* <= 5% of the pulse amplitude ± 10 mV.

2 ADJUSTMENT PROCEDURE

CONTENTS

INTRODUCTION

This procedure is based on a one channel instrument and includes directions for two channel instruments

It is not always necessary to perform the entire adjustment procedure. Adjust only those sections which have failed a performance test.

SAFETY

The HP 8160A is a Safety Class 1 instrument.

It has an exposed metal chassis that is directly connected to earth potential through the line power cord.

Before adjusting the instrument review:

1. The Safety Summary, page ix (red page)
2. The Instrument Reference Manuals
3. The instrument safety markings.

ADJUSTMENT PROCEDURE NOTES

(A/B) AND (A,B)

(A/B) = either A or B.
(A,B) = both A and B.

Cables

BNC to BNC cables are not listed in the adjustment procedures equipment lists, but they must meet the specifications in Appendix B, Recommended Test Equipment. They will be referred to as BNC cables in the adjustment procedure.

SMB to BNC cable, HP Part Number 08160-61610.

a. When it is part of the instrument's original hardware, it is called an instrument cable.
b. Non-instrument cables are called test cables.

Keep all cable lengths to a minimum.

Component Layout Diagrams

Component layout diagrams show the adjustment point locations as well as the circuit components.

Configuration, Instrument

All boards must be installed in the instrument when performing an adjustment procedure unless otherwise specified.

Connection Board

Printed circuit board 08160-66571 is referred to as the coupling board or connecting board.

Electro-Static Discharge

The HP 8160A contains components that are susceptible to ESD damage. Protective measures must be taken during installation, operation, and sevice .

Feedthrough, 50 OHM

Feedthroughs should be checked for specification compliance before performing a procedure.

Galvanic Seperation

Galvanic seperation is accomplished by using an isolation transformer.

Impedance Matching

Impedance matching must be observed in the adjustment procedure:

NOTE: All load and source impedances are 50 ohm unless otherwise stated.

1. The SMB to BNC cables and the connecting boards have 50 ohm signal lines.
2. The instrument has 50 ohm and 1 k ohm output modes.
3. The external input has 50 ohm or 10 k ohm input impedamce capability.
4. Some test equipment has variable impedance capability.
5. Many test steps require the use of 50 ohm terminations.

Power Supply Adjustments

An isolation transformer must be used when adjusting the power supply.

Pulse Generator

"Pulse generator" will always refer to a piece of test equipment in the adjustment procedure.

The HP 8160A will always be called the HP 8160A.

Switch Settings

Normal operating mode switch settings:

1. Delay/Width Switches
   a. A128/S1 = Delay
   b. A228/S1 = Width
   c. A328/S1 = Delay (OPTION 020)
   d. A428/S1 = Width (OPTION 020)
2. Channel Address Switches
   a. A128/S2 = 1
   b. A228/S2 = 1
   c. A328/S2 = 2 (OPTION 020)
   d. A428/S2 = 2 (OPTION 020)
3. Channel Switches.
   a. A140/S1 = 'A'
   b. A240/S1 = 'B'
   c. A150/S1 = 'A'
   d. A250/S1 = 'B'

Test Equipment, Recommended

The recommended test equipment is listed in Appendix A.

Transition Times

All transition times are minimum unless otherwise stated.

VARIAC

"VARIAC" means variable alternating current power supply.

Warm-up Period

Warm-up the instrument at the bench for 45 minutes with the top cover on before beginning a procedure.

Keep the top cover on the instrument between adjustments.

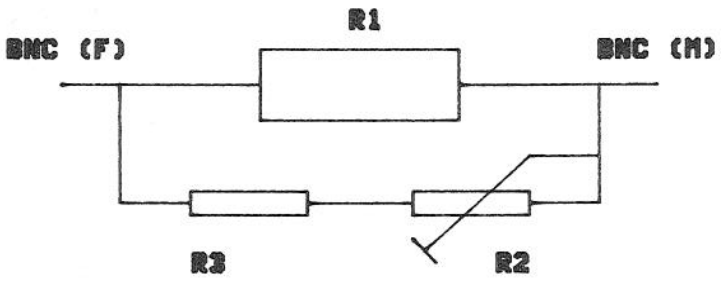
50 ohm/20 dB TEE

The "50 ohm/20 dB TEE" is a sampling scope T adapter fitted with a 50 ohm termination and a 20 dB Attenuator.

50 OHM, 0.1%, 10 W FEEDTHROUGH TERMINATION

This feedthrough must be used only where specified for DC voltage measurements.

The following figure provides a schematic and a parts list except for the case. The case must provide shielding and maintain grounding integrity.



R1 = 53.6 ohm, 1%, 10 W;
HP Part Number: 0699-0146.
R2 = 200 ohm, 10%, 0.5 W, Variable trimmer;
HP Part Number: 2100-3350.
R3 = 681 ohm, 1%, 0.5 W;
HP Part Number: 0757-0816.
BNC (M): HP Part Number: 1250-0045.
BNC (F): HP Part Number: 1250-0083.

1. DUTY CYCLE AND VOLTAGE LEVEL ADJUSTMENTS

This procedure consists of four parts:

1. Power Supply Module Removal.
2. Minimum Duty Cycle Adjustment.
3. Maximum Duty Cycle Adjustment.
4. Voltage Adjustments.

WARNING

Read the WARNING notice on the rear panel before beginning the Duty Cycle and Voltage Level Adjustments.

Hazardous voltages are present. Service must be performed only by qualified personnel.

PART 1: POWER SUPPLY MODULE REMOVAL.

1. Disconnect the line voltage power cord from the instrument.
2. Remove three feet: two from the end frame at the top cover and the foot near the power line selector. Carefully remove the top cover; avoid damaging the top cover's RFI shielding.
3. Remove the three screws securing the power supply module: they are marked by white circles and the ATTENTION message.
4. WARNING-the power supply module may be hot. Slide the module out of the chassis; avoid damaging the RFI shielding, the fan cord, and A11/J1.

PART 2: MINIMUM DUTY CYCLE ADJUSTMENT.

EQUIPMENT:

1. DC Power Supply, 0-60 VDC, leads
2. Realtime Oscilloscope and one 10:1 probe.

SET-UP:

1. Remove A11 from the module.
2. Disconnect wires 1 and 5.
3. Leave wires 3 and 8 connected to chassis mounted A11/R137.
4. Connect the DC Power supply.
   a. Negative pole (-) to A11/TP10.
   b. Positive pole (+) to the anode of A11/CR108.
5. Set the power supply: 40 VDC
6. Set Scope: Time base = 1 us/div.
7. Connect the scope probe (10:1) to A11/TP4.

ADJUSTMENT PROCEDURE:

1. Increase the DC power supply voltage until the oscillation stops.
2. Decrease the voltage until the oscillation just starts.
3. Adjust A11/R101 for a positive pulse width of 1.25 us +0.40, - 0.25 us.
4. Disconnect the power supply.
5. Reconnect wires 1 and 5.

PART 3: MAXIMUM DUTY CYCLE ADJUSTMENT.

NOTE: **This adjustment must be done with a line voltage of 115 VAC, and the instrument's line fuse must be 8 A.**

EQUIPMENT:

1. Variac
2. Isolation Transformer
3. Realtime Oscilloscope and one HV probe
4. Line Fuse, 115 VAC/8 AMPERE
5. Extender Board (08160-66574)-Mother Board
6. Extender Board (08160-66577)-Regulator Board.

SET-UP:

1. Place A11 on the regulator extender board.
2. Install a 115 VAC/8 A fuse in the instrument.
3. Set the line voltage selector to 115 VAC
4. Connect the power supply mother board, A10, with the instrument mother board, A1, via extender board 08160-66574.
5. Connect the variac power cord to the power supply module, and raise the variac voltage to 115 VAC.

   NOTE: Use an isolation transformer to isolate the variac from the line power.

6. Set power supply module line switch to **ON**.
7. Set scope: 2 us/div.

ADJUSTMENT PROCEDURE:

1. Connect the oscilloscope HV probe to heat sink, A11/MP1, which is a common point between the collectors of A11/Q101 and A11/Q102.
2. Reduce the variac voltage until the jitter at the trailing edge begins to stop.
3. Adjust the scope's time base for sweep for a full scale display of one period.
4. Adjust A11/R140 for a 45% ± 1% duty cycle.

PART 4 VOLTAGE ADJUSTMENTS.

SET-UP:

Set variac: 92 VAC. NOTE: Use an isolation transformer to isolate the variac from the line power.

ADJUSTMENT PROCEDURE:

1. Measure +5Vfx and -5Vfx with the Multimeter (see Table 5-2.1 for TPs).
2. Connect the Multimeter to the TP in **STEP 1** with the lowest absolute value.
3. Adjust A11/R102 to an absolute value of 6.36V +10mV -0mV.
4. Check the voltages in the following table.
5. Replace the power supply module.

VOLTAGE	LOW LIMIT (OPTION 020)	HIGH LIMIT (STANDARD)	V-TP (A10/J1) PIN	GND-TP (A10/J1 PIN
FIXED VOLTAGE SUPPLIES:				
+5Vfx	=>6.36V	<= 7.0V	6,7	1
-5Vfx	<=-6.36V	=>-7.0V	4,5	2
+12Vfx	=> 13.0V	<= 16.0V	9	1
-12Vfx	<=-13.0V	=>-16.0V	10	2
+20Vfx	=> 21.5V	<= 25.0V	8	1
-20Vfx	<=-21.5V	=>-25.0V	3	2
FLOATING VOLTAGE SUPPLIES:				
+5Vfl	=> 6.7V	<= 8.0V	13	15
-5BVfl	<= 6.75V	=>-8.0V	12	15
+20Vfl	=> 21.5V	<= 25.0V	14	15
-20Vfl	<=-21.5V	=>-25.0V	11	15

2. VOLTAGE REGULATOR ADJUSTMENTS.

This procedure consists of two parts:

1. Fixed Voltage adjustments
2. Floating Voltage Adjustments.

EQUIPMENT:

1. Multimeter with floating inputs
2. Isolation Transformer
3. Line fuse (115 VAC/8 A or 230 VAC/4 A)

SET-UP:

1. Set the line voltage selector switch and connect the instrument to the line power. NOTE: Use an isolation transformer to isolate the instrument from the line power.
2. The test points are located on the top, right, rear corner of the mother board.
   NOTE: The side panel can easily be removed for easier access to the Test Points with dual channel instruments.

PART 1 FIXED VOLTAGE ADJUSTMENTS.

SET-UP:

Connect the Multimeter LO (common) to the **FIXED GROUND** test point.

ADJUSTMENT PROCEDURE:

1. Connect Multimeter HI (input) to +5 Vfx test point.
2. Adjust A18/R95 to 5.000 V ± 10 mV.
3. Measure -5Vfx. It shoud be -5.000 V ± 30 mV
4. Connect Multimeter Hi (input) to +20 Vfx test point.
5. Adjust A18/R50 to 20.000 V ± 20 mV.
6. Connect Multimeter Hi (input) to -20 Vfx test point.
7. Adjust A18/R71 to -20.000 V ± 20 mV.

PART 2 FLOATING VOLTAGE ADJUSTMENTS.

SET-UP:

Connect the Multimeter Lo (common) to the **FLOATING GROUND** test point.

ADJUSTMENT PROCEDURE:

1. Measure +5 Vfl. It should be 5.000 V ± 30 mV.
2. Measure -5 Vfl. It should be -5.000 V ± 30 mV.
3. Connect Multimeter Hi (input) to +20 Vfl test point.
4. Adjust A18/R223 to 20.000 V ± 20 mV.
5. Connect Multimeter Hi (input) to -20 Vfl testpoint.
6. Adjust A18/R243 to -20.000 V ± 20 mV.

3. SHIFT VOLTAGE ADJUSTMENT.

EQUIPMENT:

1. Multimeter with floating inputs
2. Isolation Transformer

SET-UP:

1. Set the line voltage selector switch, and connect the instrument to the line power. NOTE: Use an isolation transformer to isolate the instrument from the line power.
2. Set HP 8160A;
   a. RCL 0
   b. HIL (A,B) = 9.99V LOL (A,B)= 0.00V.
3. Connect Multimeter.
   a. LO (Common) to fixed ground.
   b. HI (Input) to floating ground.

ADJUSTMENT PROCEDURE:

1. Adjust A150/R15 to 10.000 V ± 50 mV.
2. Set HP8160A.
   HIL (A,B) = 1 V and LOL (A,B) = -1 V.
3. Multimeter must read 0.000 V ± 200 mV.

4. REPETITION RATE GENERATOR ADJUSTMENT.

EQUIPMENT:

1. Multimeter.
2. Counter.
3. Cable (08160-61610)
4. Extender Board (08160-66573).
5. Extender Boards, two each, (08160-66572).
6. Drawing: #13, page 8-92.

SET-UP:

1. Remove the two coupling PCBs that connect A23 to A20.
2. Place A23 on extender board 08160-66573.
3. Insert extender boards, 08160-66572, into A20/J8 and A20/J9.
4. Reconnect A20 and A23 with the two coupling PCBs.
5. Connect A23/J5 via cable 08160-61610 and a BNC to BNC cable to the counter's Channel A input.

ADJUSTMENT PROCEDURE:

1. Set HP 8160A.
   a. PER = 100 ns
   b. WID (A,B) = 8 ns
   c. DEL (A,B) = 0 ns
   d. LEE (A,B) = 3 ns TRE (A,B) = 3 ns
2. Connect Multimeter:
   a. LO (common) to A23/TP4, fixed ground.
   b. HI (input) to A23/TP5.
3. Adjust A23/R141 for -5 V ± 20 mV.
4. Set HP 8160A: PER = 99.9 ns.
5. Adjust A23/R159 for -500 mV ± 2 mV.
6. Repeat steps 1-5 until the voltages are within tolerance. Then remove the Multimeter Probes.
7. Set counter for a period measurement.
   a. FUNCTION = PERIOD A.
   b. Channel A INPUT = 50 ohm, X1, DC.
   c. INPUT MODE = SEP (SEPERATE).
8. Set HP 8160A: PER = 999 ns
9. Adjust A23/R141 for 999 ns ± 3 ns.
10. Set HP 8160A: PER = 100 ns
11. Adjust A23/R79 for 99.5 ns ± 0.3 ns.
12. Repeat steps 8-11 until the periods are within tolerance.

13. Set the HP 8160A: PER = 200 ns.
14. Record the reading and calculate the percentage (%) of error.
15. Adjust A23/R159 for a reading of 200 ns + 1.5 x % error
    NOTE: The error was measured and calculated in steps 13 and 14.
16. Repeat Steps 8-12.

17. **PRESET** A23/R74, A23/R78, and A23/C19 to their mid-range positions.

18. Set HP 8160A: PER = 99.9 ns.
19. Adjust A23/C21 for 99.9 ns ± 0.3 ns.
20. Set HP 8160A: PER = 20 ns
21. Adjust A23/R78 for 20 ns ± 0.1 ns.
22. Repeat steps 14 and 17 until the periods are within tolerance.

23. Measure the HP 8160A period at PER 20 ns and PER 35 ns and, record the readings.

    Calculate the period error.
    a. If the error at 20 ns is higher:
        1.) Set HP 8160A: PER = 20 ns.
        2.) Adjust A23/R78 for 20 ns ± 0.2 ns.
    b. If the error at 35 ns is higher:
        a.) Set HP 8160A: PER = 35 ns.
        b.) Adjust A23/R74 for 35 ns ± 0.3 ns.

24. Repeat step 19 until: PER 20 ns setting = 20 ns ± 0.3 ns
    PER 35 ns setting = 35 ns ± 0.45 ns.

25. Set HP 8160A: PER = 99.9 ns.
26. Adjust A23/C21 for 99.0 ns ± 0.3 ns.
    NOTE: This adjustment allows for the thermal change which occurs when the board is replaced into the instrument.

27. Re-assemble the instrument and replace the top cover.

28. Allow a 20 minute warm-up period.

29. Connect the HP 8160A's OUTPUT to the counter's channel A input.
30. Measure the period accuracy.
    a. For the range < 100 ns, the accuracy must be ± 2.0 % of the programmed value ± 0.2 ns at 25 degrees C.
    b. For the range > 100 ns, the accuracy must be ± 1.5 % of the programmed value at 25 degrees C.

31. Repeat Steps 8-30.

5. RATE CLAMP ADJUSTMENT.

EQUIPMENT:

1. Pulse Generator.
2. Sampling oscilloscope, 50 ohm/20 dB TEE
3. Cable (08160-61610).
4. Extender Board 08160-66573

SET-UP:

1. Place A23 on an extender board; it is not necessary to connect A23 to A20 via the connecting PCBs.
2. Set scope.
   a. Time base = 20 ns/div.
   b. Vertical sensitivity = 20 mV/div.
3. Set Pulse Generator.
   a. Squarewave.
   b. Period = approximately 300 ns.
   c. Amplitude = 3 V.
   d. Offset = 0 V.
4. Set HP 8160A.
   a. INPUT MODE = GATE.
   b. EXT SLOPE = POS.
   c. EXT INPUT SWITCH = 50 ohm.
   d. PER = 30 ns.
5. **PRESET** A23/R57 fully CW.
6. CONNECT A23/J5 via a test cable and a 50 ohm/20 dB TEE to the scope's Channel A input.
7. Connect the pulse generator's output to the HP 8160A's EXT INPUT.
8. Connect the pulse generator's trigger output to the scope's trigger input.
9. Adjust the HP 8160A EXT INPUT trigger level.

ADJUSTMENT PROCEDURE:

1. Adjust A23/R57 CCW for a minimum delay at the leading edge of the first pulse.
2. **SET REFERENCE:** Position the leading-edge of the first pulse at the center vertical-line of the scope's display.
3. Adjust A23/R57 CW until the intervals between the three pulses are as short as possible and still equal.
   NOTE: The first pulse's delay time must not increase.

6. DELAY AND WIDTH PRE-ADJUSTMENTS.

The Delay and Width Pre-adjustments are only performed when there is:

1. A specific problem in a TI 1, TI 2, or TI 3 circuit
2. A failure in the Delay and Width Final Adjustments Procedure, Procedure 13.

The Time Interval Adjustment Procedure consists of five parts:

1. SIGNAL OUT Adjustment.
2. Delay Adjustment.
3. Width Adjustment.
4. Reference Trigger Adjustment.
5. Long Delay Adjustment.
6. Minimum Delay Adjustment.

EQUIPMENT:

1. Sampling Oscilloscope, 50 ohm/20 dB TEE, and 1:1 Probe tip.
2. Counter
3. Cables, two each, 08160-61610.
4. Extender board 08160-66573
5. Extender board 08160-66572

PART 1 "SIGNAL OUT" ADJUSTMENT.

SET-UP:

1. Set HP 8160A as follows:
   a. PER = 100 ns.
   b. DEL (A,B) = 0 ns
      WID (A,B) = 8 ns
      LEE (A,B) = 3 ns
      TRE (A,B) = 3 ns
      HIL (A,B) = 2.8 V
2. Set scope: Horizontal sensitivity = 0.5 ns/div.
3. Set DELAY/WIDTH switches as follows:
   a. A128/S1 to DELAY, position #2.
   b. A228/S1 to DELAY, position #2.
   c. A328/S1 to DELAY, position #2, OPTION 020.
   d. A428/S1 to DELAY, position #2, OPTION 020.
4. Set the Channel Address switches as follows:
   a. A128/S2 to address #1.
   b. A228/S2 to address #2.
   c. A328/S2 to address #1, OPTION 020.
   d. A428/S2 to address #2, OPTION 020.
5. Turn the instrument off and then on.
   NOTE: The power cycling is needed to allow the instrument to identify its new configuration. If a power loss occurs during the procedure, the entire procedure must be repeated.
6. Connect HP8160A TRIG OUTPUT to the scope's external trigger input.

ADJUSTMENT PROCEDURE:

1. With the sampling scope's 1:1 probe, probe the **WIDTH TRIGGER OUT** signal line on the A126/A127 connecting PCB, 08160-66571.
2. **SET REFERENCE:** Adjust the scope delay so the pulse's leading-edge (50% point) is aligned with the center vertical-line of the scope's display.
3. Probe the **SIGNAL OUT** signal line on the connecting PCB.
4. Adjust A126/R138 for 0 ns ± 50 ps difference between the pulse's leading edge 50% point and the center graticule.
5. Repeat steps 1-4 for the A226, A227, and A228 boards.
6. Repeat steps 1-4 for the A326, A327, and A328 boards, OPTION 020.
7. Repeat steps 1-4 for the A426, A427, and A428 boards, OPTION 020.

PART 2 DELAY ADJUSTMENT.

SET-UP:

Connect A128/J5 via a 50ohm/20 dB TEE to scope's input.

ADJUSTMENT PROCEDURE:

1. Set HP8160A: DEL A = 20 ns DEL B = 0 ns.
2. Set A128/S1 to Width.

3. SET REFERENCE: Align the pulse's leading-edge (50 % point) with the center verticle-line of the scope's display.
4. Set A128/S1 to the Delay position.
5. Set HP 8160A to: DEL A = 0 ns DEL B = 0 ns.
6. Adjust A128/R219 for 0 ns ± 50 ps between the pulse's leading edge 50% point and center graticule.

7. Set HP8160A to: DEL A = 0 ns DEL B = 20 ns.
8. Repeat steps 2-6 for A228.

9. Repeat steps 1-6 for A328, OPTION 020.

10. Set HP8160A to: DEL A = 0 ns DEL B = 20 ns.
11. Repeat steps 2-6 for A428, OPTION 020.

PART 3 WIDTH ADJUSTMENTS.

ADJUSTMENT PROCEDURE:

1. Set HP8160A to: DEL A = 20 ns DEL B = 0 ns.
2. SET REFERENCE: Align the pulse's leading-edge (50% point) with the vertical center-line of the scope's display.
3. Set A128/S1 to the Width position.
4. Adjust A128/R239 for 0 ns +300ps/-50ps between the pulse's trailing-edge (50% point) and the reference.
5. Set A128/S1 to the Delay position.

6. Set HP8160A to: DEL A = 0 ns DEL B = 20 ns.
7. Repeat steps 2-5 for A228.

8. Repeat steps 1-5 for A328, OPTION 020.

9. Set HP8160A to: DEL A = 0 ns DEL B = 20 ns.
10. Repeat steps 2-5 for A428, OPTION 020.

PART 4 REFERENCE TRIGGER ADJUSTMENT.

SET-UP:

1. Set Channel Address Switches.
   a. A128 = 1.
   b. A228 = 1.
   c. A328 = 2, OPTION 020.
   d. A428 = 2, OPTION 020.
2. All Delay/Width switches should be in the Delay position.
3. Connect A128/J5 via a 50 ohm/20 dB TEE to the scope's input.
4. Connect A23/J5 to the scope's trigger input.
   NOTE: The cables in 3. and 4. must be the same length.

ADJUSTMENT PROCEDURE:

1. Set HP8160A to: DEL A = 0 ns DEL B = 0 ns.
2. SET REFERENCE: Align the pulse's leading edge (50% point) with the vertical center-line of the scope's display.
3. Disconnect the instrument cable form A127/J5.
4. Switch test cable 08160-61610 from A128/J5 to A127/J5.
5. Adjust A127/R112 for 0 ns +50 ns/- 300 ns between the pulse's leading-edge (50% point) and the reference.
6. Disconnect the test cable from A127/J5.
7. Reconnect the instrument cable to A127/J5.

8. Repeat Part D for A227/A228 by adjusting A227/R112.

   NOTE: If A128 and A228 are replaced by A328 and A428, remember to perform the Reference Trigger Adjustment.

PART 5 LONG DELAY ADJUSTMENT.

SET-UP:

1. Remove the connector PCB from A127 and A128.
2. Put A128 on extender board 08160-66573.
3. Insert extender board 08160-66572 into A127/J6.
4. Reconnect A127 and A128 with the connector PCB.
5. Connect HP8160A TRIG OUTPUT to the scope's trigger input.

ADJUSTMENT PROCEDURE:

1. Set Channel address switches.
   a. A128 = 1
   b. A228 = 2
   c. A328 = 1, OPTION 020.
   d. A428 = 2, OPTION 020.

2. Set HP8160A to:
   a. PER = 400 ns.
   b. DEL A = 200 ns DEL B = 0.0 ns.

3. Connect the sampling scope's 1:1 probe across A128/R26.
4. Adjust A128/R37 so the switching spike occurs from 18-20 ns after the pulse's falling edge (50% point).
5. Disconnect scope probe.

6. Set HP8160A to:
   a. PER = 2 ms.
   b. DEL A = 1 ms DEL B = 0 ms.
7. Set A128/S1 to the Width position.
8. Set counter to:
   a. Trig level A = -0.3 V and adjust for stable count.
   b. Trig level B = +0.3 V and adjust for stable count.
   c. Input Mode = Com.
   d. Channel A/B = 50 ohm.
9. Connect A128/J5 to the counter's input.
10. Adjust A128/C10 for 1.0014 ms ± 0.0005 ms.

11. Set A128/S1 to Delay.
12. Replace A128 into the instrument.

13. Repeat steps 2-12 with A228, but substitute the following:
    a. Step 2 Set HP 8160A: DEL A = 0 ns DEL B = 200 ns.
    b. Step 6 Set HP 8160A: DEL A = 0 ms DEL B = 1 ms.

14. Repeat steps 2-12 with A328 , OPTION 020.

15. Repeat step 13 with A428, OPTION 020.

PART 6 MINIMUM DELAY ADJUSTMENT.

SET-UP:

1. Set the Channel address switches.
   a. A128 = 1
   b. A228 = 2
   c. A328 = 1 (OPTION 020)
   d. A428 = 2 (OPTION 020)
2. Set all Delay/Width switches to DELAY.
3. Set scope.
   a. Time base = 1 ns/div.
   b. Vertical Sensitivity = 100 mV/div.
4. Set HP 8160A.
   a. PER = 100 ns
   b. DEL A = 0 ns DEL B = 0 ns.
5. Connect A128/J4 via a 50 ohm/20 dB TEE to the sampling scope's input.
6. Connect the HP 8160A's TRIG OUTPUT to the scope's trigger input.

ADJUSTMENT PROCEDURE:

1. Check HP 8160A DEL A from 0.0 ns to 0.9 ns in 0.1 increments. The measurements must be made at the pulse's leading edge 50% point.
2. Change A126/C8 (factory select value, 0-10 pF) if DEL A = 0.5 ns is out of specification.
3. Set scope: Time base = 2 ns/div.
4. Set the HP 8160A as follows and make the adjustment required:
   a. Set DEL A = 1 ns Adjust A126/R151 check for 1 ns nominal
   b. Set DEL A = 2 ns Adjust A126/R153 check for 2 ns nominal
   c. Set DEL A = 3 ns Adjust A126/R155 check for 3 ns nominal
   d. Set DEL A = 4 ns Adjust A126/R157 check for 4 ns nominal

   The measurements must be made at the pulse's leading edge 50% point.
5. Check HP 8160A DEL A from 0 ns to 50 ns in 5 ns increments.
6. Repeat steps 1-5 for A228/A226 and DEL B.
7. Repeat steps 1-5 for A328/A326 and DEL A, OPTION 020.
8. Repeat steps 1-5 for A428/A426 and DEL B, OPTION 020.
9. Set Delay/Width to their normal operating positions.
10. Set Channel address to their normal operating positions.
11. Turn the HP8160A power off and then on again.

7. SLOPE GENERATOR ROLL-OFF ADJUSTMENT.

When the slope generator is adjusted, do the following also:

1. Slope Generator Roll-off Check, Amplitude, and Offset Adjustments
2. Output Amplifier Symmetry, Offset, Gain Adjustments.

EQUIPMENT:

1. Realtime Oscilloscope and a 10:1 probe.
2. Cable 08160-61610.
3. Extender Board 08160-66573.

SET-UP:

1. Place A140 on extender board.
2. Scope settings:
   a. Time base = 10 us
   b. Channel A = 200 mV/DIV
   c. Channel B = 50 mV/DIV
   d. ALT
   e. DC
   f. EXT TRIG.

3. Set HP 8160A.
   a. PER = 100 us
   b. WID (A/B) = 50 us
   c. DEL (A/B) = 0.0 ns
   d. LEE = (A/B) 5 us TRE (A/B) = 5 us
   e. HIL = (A/B) +1 V LOL (A/B) = -1 V

4. Connect A140/J5 via a test cable and a 50 ohm feedthrough termination to the scope's Channel A input.
5. Connect HP8160A TRIG OUTPUT to the scope's trigger input.
6. Connect the 10:1 probe to the scope's Channel B input.

ADJUSTMENT PROCEDURE:

1. **PRESET** A140/R127 fully CCW.
2. **PRESET** A140/R142 fully CW.
3. Adjust the scope's vertical sensitivity for a six division peak-to-peak pulse, and center the pulse on the center horizontal axis.

4. Connect the 10:1 probe to the cathode of A140/CR8.
5. Turn A140/R127 fully CW.
6. Turn A140/R142 fully CCW.
7. Align the CH B waveform so it overlays the waveform of CH A.

8. Adjust A140/R127 so the Channel B signal has approximately 3% greater amplitude then the Channel A signal at the high level.
9. Adjust A140/R142 so the Channel B signal has approximately 3% greater amplitude then the Channel A signal at the low level.

10. Repeat steps 1-9 for A240, OPTION 020.

8. SLOPE GENERATOR ROLL-OFF CHECK, AMPLITUDE, AND OFFSET ADJUSTMENTS.

This procedure consists of three parts:

1. Roll-off check
2. Amplitude adjustment
3. Offset adjustment

EQUIPMENT:

1. Multimeter
2. Cables, 2 each, 08160-61610
3. 50 ohm feed through termination, 2.0 %, 2 W
4. 50 ohm feed through termination, **0.1%, 10 W**
5. BNC to dual banana plug adapter.
6. Extender board, 08160-66573

PART 1 ROLL-OFF CHECK

SET-UP:

1. Place A140 on the extender board.
2. Connect A140/J4 via cable 08160-61610 to a 50 ohm, 2 W, feed through termination.
3. Connect A140/J5 via a 50 ohm, **0.1%, 10 W**, feedthrough termination and a BNC to dual banana plug adapter to the Multimeter's inputs.
4. Connect the HP 8160A's TRIG OUTPUT to the Multimeter's trigger input.

ADJUSTMENT PROCEDURE:

1. SET HP 8160A.
   a. PER = 100 ms
   b. WID (A/B) = 50 ms
   c. DEL (A/B) = 30 ms
   d. TRE (A/B) = 50 us

2. Set Multimeter
   a. SGL TRIG.
   b. Blue/AUTO ZERO = Auto Zero Off
   c. Blue/4 = 4 digits

3. Set HP 8160A: LEE (A/B) = 99.9 us.
4. Record Multimeter reading (high level).

5. Set HP 8160A: LEE (A/B) = 100.0 us.
6. Record Multimeter reading (high level).

7. The difference between the readings at step 4 and 6 should be < ± 5 mV.

8. Set HP 8160A.
   a. DEL (A/B) = 80 ms
   b. LEE (A/B) = 50 us.

9. Set HP 8160A: TRE (A/B) = 99.9 us.
10. Record Multimeter reading (low level).

11. Set HP 8160A: TRE (A/B) = 100 us.
12. Record the Multimeter reading (low level).

13. The difference between the reading at steps 10 and 12 must be < ± 5 mV.

14. If the limits are not met, repeat Section 5-2.8 using 4% instead of 3%.

15. If the limits are not met using 4%:
    1. Perform the Roll-off Calibration Procedure on the following page.
    2. Repeat the Roll-off Adjustment Procedure using 3%.

16. Repeat Part 1 for A240, OPTION 020.

ROLL-OFF CALIBRATION PROCEDURE

This procedure is only performed when the Roll-off Check on the preceeding page fails.

EQUIPMENT:

1. Realtime Scope and a 10:1 probe
2. Test Cable 08160-61610
3. Extender Board 08160-66573
4. Drawing 21, page 8-126.

SET-UP:

1. Place A140 on an extender board.
2. Scope Settings:
   a. Time base = 10 us
   b. Channel A = 200 mV/division
   c. Channel B = 50 mV/division
   d. ALT
   e. DC
   f. EXT TRIG

3. Set HP 8160A:
   a. PER = 100 us
   b. WID (A/B) = 50 us
   c. DEL (A/B) = 0.0 ns
   d. LEE (A/B) = 5 us TRE (A/B) = 5 us
   e. HIL (A/B) = +1 V LOL (A/B) = -1 V

4. Connect A140/J5 via a test cable and a 50 ohm termination to the scope's Channel A input.

5. Connect A140/J4 via a test cable to a 50 ohm termination.

6. Connect the HP 8160A's TRIG OUTPUT to the scope's trigger input.

7. Connect the 10:1 probe to the scope's Channel B input.

8. Connect the probe to A140/U29 pin 16 or A140/CR8's cathode.

CALIBRATION PROCEDURE:

1. Adjust A140/R127 and A140/R142 for minimum signals.

2. By selecting the correct value for R248* (factory select value), align the Chanel B waveform so that it overlays the Channel A waveform.

PART 2 AMPLITUDE ADJUSTMENT.

ADJUSTMENT PROCEDURE:

1. SET HP 8160A.
   a. PER = 100 ms
   b. DEL (A/B) = 80 ms
   c. WID (A/B) = 50 ms
   d. LEE (A/B) = 5 us TRE (A/B) = 5 us
2. Record the DVM reading as V NORM (high level); save for Section 5.2.10.

3. Change cable at A140/J5 to A140/J4.
4. Set HP 8160A: DEL (A/B) = 30 ms.
5. Record the DVM reading as V COMP (high level); save for Section 5.2.10.

6. Calculate V (high level) from the following formula:

$$\text{V (high level)} = \frac{\text{V NORM (high level)} + \text{V COMP (high level)}}{2}$$

7. Adjust A140/R207 to V (high level) ± 5 mV.

8. Repeat steps 1-7 until V (NORM) = V (COMP).

9. Set HP 8160A: DEL (A/B) = 80 ms.
10. Record the DMV reading as V COMP (low level); save for Section 5-2.10.
11. Connect the cable at A140/J4 to A140/J5
12. Set HP 8160A: DEL (A/B) = 30 ms.
13. Record the DMV reading as V NORM (low level); save for Section 5-2.10.

PART 3 OFFSET ADJUSTMENT.

ADJUSTMENT PROCEDURE:

14. Calculate V (low level) from the following formula:

    V (low level) = V (high level) - 1.25 V.

15. Adjust A140/R251 to V (low level) ± 5 mV.

16. Repeat steps 1-15 for A240, OPTION 020.

9. SLOPE GENERATOR RISETIME ADJUSTMENT.

NOTE: The Voltages used in step 7 calculations are obtained from the Slope Generator Amplitude Adjustment.

EQUIPMENT:

1. Counter
2. Sampling Oscilloscope, 50 ohm/20 dB TEE
3. Time Interval Probes and Time Interval Probe Adapter
4. Cable 08160-61610
5. Extender Board 08160-66573

SET-UP:

1. Place A140 on an extender board.
2. Connect Time Interval Channel A probe to a TI probe adapter.
3. Attach a 50 ohm termination to the TI probe adapter.
4. Connect cable 08160-61610 to the TI probe adapter.
5. Connect the TI Probes' rear panel START output to the counter's Channel A input.
6. Connect the TI Probes' rear panel STOP output to the counter's Channel B input.
7. Set Time Interval Probes.
   a. Set START channel to 'A + XX.X POSITIVE SLOPE'. (XX.X = 10% level).

$$10\%\ \text{level} = \frac{\text{V NORM (low level)} + \text{V COMP (low level)}}{2} + 0.125$$

   b. Set STOP channel to 'A + YY.Y POSITIVE SLOPE'. (YY.Y = 90% level).

$$90\%\ \text{level} = \frac{\text{V NORM (high level)} + \text{V COMP (high level)}}{2} - 0.125$$

8. Set counter.
   a. FUNCTION = TI A to B
   b. Channel A/B = 50 ohm, slope +, X1, DC
   e. CHANNEL A/B Trigger levels = Preset
   f. INPUT MODE = SEP (SEPERATE)

9. CALIBRATE the time interval probes.
   Perform the LEVEL operation; hold the CAL switch in the LEVEL position until the channel LEDS are on.

   NOTE: Perform the calibration with the TEE, 50 ohm termination, and the cable attached.

10. Connect cable 08160-61610 which is attached to the TI TEE to A140/J5.

ADJUSTMENT PROCEDURE:

1. Set the HP 8160A.

   a. PER = 600 us
   b. WID (A,B) = 300 us.

2. Set the HP 8160A (A,B) as follows and record the counter readings.

a.	PER = 600 us	WID = 300 us	LEE = 5.00 us	TRE = 99.9 us
b.	PER = 6ms	WID = 3 ms	LEE = 50.0 us	TRE = 999 us
c.	PER = 60 ms	WID = 30 ms	LEE = 0.50 ms	TRE = 9.99 ms
d.	PER = 600 us	WID = 300 us	LEE = 99.9 us	TRE = 5.00 us
e.	PER = 6 ms	WID = 3 ms	LEE = 999 us	TRE = 50.0 us
f.	PER = 60 ms	WID = 30 ms	LEE = 9.99 ms	TRE = 0.50 ms

3. Compare the absolute values of the counter measurements from 2a, 2b, and 2c and set the HP 8160A's LEE and TRE parameters with the settings related to this middle value.
4. Adjust a140/R83 to 5025 nominal (disregard the decimal point).

5. Compare the absolute values of the counter measurements from 2d, 2e, and 2f and set the HP 8160's LEE and TRE parameters with the settings related to this middle value.
6. Adjust A140/R113 to 1002 nominal (disregard the decimal point).

7. Set Time Interval Probes.
   a. Start channel = 'A + YY.Y NEGATIVE SLOPE'
   B. Stop channel = 'A + XX.X NEGATIVE SLOPE'

8. Repeat steps 1-6, but now compare and adjust as follows:
   a. In steps 3&4 Compare 2d,e,f Adjust A140/R41
   b. In steps 5&6 Compare 2a,b,c Adjust A140/R196.

9. Set HP 8160A.
   a. PER = 60 us
   b. WID (A/B) = 30 us
   c. LEE (A/B) = 500 ns
   d. TRE (A/B) = 9.99 us

10. Set Time Interval probes.
   a. Start channel = 'A + XX.X POSITIVE SLOPE'
   B. Stop channel = 'A + YY.Y POSITIVE SLOPE'

11. Check:
   a. LEE (A/B) = 500 ns ± 5 ns
   b. LEE (A/B) = 9.99 us ± 100 ns.

12. Set Time Interval probes.
   a. Start Channel = 'A + YY.Y NEGATIVE SLOPE'
   B. Stop Channel = 'A = XX.X NEGATIVE SLOPE'

13. Set HP 8160A.
   a. LEE (A/B) = 9.99 us
   b. TRE (A/B) = 500 ns

14. Check:
   a. TRE (A/B) = 9.99 us ± 100 ns
   b. TRE (A/B) = 500 ns ± 5 ns

15. If reading in steps 11 and 14 are out of tolerance, change A140/C25 (factory select value, 0-140 pF).

16. Repeat steps 1-15 for A240, OPTION 020.

17. Connect A140/J4 via a test cable and a 50 ohm/20dB TEE to the scope's input.
18. Connect HP 8160A TRIG OUTPUT to the scope's trigger input.

19. Set HP 8160A.
    a. PER = 600 ns
    b. WID (A/B) = 300 ns
    c. LEE (A/B) = 99.9 ns TRE (A/B) = 99.9 ns
20. Adjust A140/C18 for 99 ns nominal leading and trailing edges.

21. Set HP 8160A.
    a. PER = 6 us
    b. WID (A/B) = 3 us
    c. LEE (A/B) = 999 ns TRE (A/B) = 999 ns
22. Adjust A140/C19 for 999 ns nominal leading and trailing edges.

23. Set HP 8160.
    a. PER = 100 ns
    b. WID (A/B) = 50 ns
    c. LEE (A/B) = 3 ns TRE (A/B) = 3 ns
24. Adjust A140/R87 for a leading edge of 4.5 ns nominal.
25. Adjust A140/R90 for a trailing edge of4.5 ns.nominal.

26. Replace A140 and reconnect the instrument cables.

27. Repeat steps 17-26 for A240, OPTION 020.

28. Replace top cover.
29. After a 20 minute warm-up period, check the slope times in Steps 20, 22, 24, and 25.

30. Perform Section 5-2.11, Amplifier Pulse Adjustment Procedure, Steps 1-19, PARTS A. B, AND C.

31. Repeat steps 29 and 30 for A240, OPTION 020.

10. OUTPUT AMPLIFIER SYMMETRY, OFFSET, GAIN, AND PULSE FLATNESS ADJUSTMENTS.

This procedure consists of four parts:

1. Symmetry Adjustment
2. Offset Adjustment
3. Gain Adjustment
4. Pulse Flatness Adjustment

NOTE: The Roll-off Adjustment must be correct before performing the output amplifier adjustment.

EQUIPMENT:

1. Sampling Oscilloscope, 50 ohm/20 dB TEE
2. Real Time Oscilloscope, 1:1 Probe
3. Multimeter
4. 50 ohm termination, 1%, 2 W
5. 50 ohm feed through, **0.1%, 10 W**
6. BNC to dual banana plug adapter

PART 1 SYMMETRY ADJUSTMENT.

SET-UP:

1. Set HP 8160A.
   a. PER = 0.5 ms
   b. WID (A/B) = 0.25 ms
   c. LEE (A/B) = 20 ns TRE (A/B) = 20 ns
   d. HIL (A/B) = +4.99 V LOL (A/B) = -4.99 V
2. Set REALTIME scope.
   a. AC coupled
   b. Time Base = 0.2 ms/div
   c. Vertical Sensitivity = 5 mV/div

ADJUSTMENT PROCEDURE:

1. With the 1:1 probe, probe A151/Q200's emitter on the circuit side of the PCB.
2. Adjust A151/R208 for a minimum signal.
3. Set HP 8160A: HIL (A/B) = + 0.49 V LOL (A/B) = - 0.49 V
4. Probe A151/Q200's emitter.
5. Adjust A151/R206 for a minimum signal.

PART 2 OFFSET ADJUSTMENT.

NOTE: Before proceeding, check pulse flatness. It must be better that 1%. If it is not, perform PART 4, Pulse Flatness Adjustment, first.

SET-UP:

1. Set Multimeter.
   a. SGL = Single Trigger
   b. Blue/Auto Zero = Auto Zero Off
   c. Blue/4 = 4 digits
2. Set HP 8160A.
   a. PER = 100 ms
   b. WID (A/B) = 50 ms
   c. HIL (A/B) = +4.99 V LOL (A/B) = -4.99 V
   d. LEE (A/B) = 20 ns TRE (A/B) = 20 ns
   e. OUTPUT MODE (A/B) = NORM
   f. DEL (A/B) = 80 ms
3. Store parameters: STO 1.
4. Set HP 8160A.
   a. DEL = 30 ms.
   b. OUTPUT MODE (A/B) = COMP
5. Store parameters: STO 2.
6. Connect the HP 8160A TRIG OUTPUT to the Multimeter's trigger input.
7. Connect the HP 8160A OUTPUT (A/B) via a 50 ohm, **10 W, 0.1%** feedthrough and a BNC to dual banana plug adapter to the Multimeter's inputs.

ADJUSTMENT PROCEDURE:

1. Recall parameter set 1, RCL 1, and record the reading as V (NORM).
2. Recall parameter set 2, RCL 2, and record the reading as V (COMP).
3. Adjust A151/R107 for <= 5 mV difference between the V (NORM) and V (COMP) readings.

4. RCL 1; set HP 8160A: HIL (A/B) = 0.5 V,LOL (A/B) = -0.5 V; record the reading.
5. RCL 2; set HP 8160A: HIL (A/B) = 0.5 V,LOL (A/B) = -0.5 V; record the reading.
6. Adjust A151/R311 for the minimum difference between the absolute value of the readings.

7. RCL 1; set HP 8160A: HIL (A/B) = 1 V,LOL (A/B) = -1 V; record the reading.
8. RCL 2; set HP 8160A: HIL (A/B) = 1 V,LOL (A/B) = -1 V; record the reading.
9. Adjust A151/R308 for the minimum difference between the absolute value of the readings.

10. RCL 1; set HP 8160A: HIL = 0.49 V,LOL = -0.49 V; record the reading.
11. RCL 2; set HP 8160A: HIL = 0.49 V,LOL = -0.49 V; record the reading.
12. Adjust A151/R289 for the minimum difference between the absolute value of the readings.
13. Repeat steps 1-12 as required to establish the minimum differences.

PART 3 GAIN ADJUSTMENT.

ADJUSTMENT PROCEDURE:

NOTEs: If a low level in steps 1-54 of PART 3 is out of limit, repeat PART 2, Offset Adjustment.

Repeat each adjustment for the best setting combination.

1. Set HP 8160A.
   a. HIL (A/B) = 3.98 V LOL (A/B) = 3.98 V
   b. OUTPUT MODE (A/B) = 1 K ohm

2. Set HP8160A: DEL (A/B) = 80 ms.
3. Adjust A151/R264: high level = 4.014 V ± 10 mV.
4. Set HP 8160A: DEL (A/B) = 30 ms.
5. Low level = -4.014 V ± 10 mV.

6. Set HP 8160A.
   a. OUTPUT MODE (A/B) = 50 ohm
   a. HIL (A/B) = 1.99 V LOL (A/B) = -1.99 V

7. Set HP 8160A: DEL (A/B) = 80 ms.
8. Adjust A151/R275 for high level = 2.000 V ± 7 mV.
9. Set HP 8160A: DEL (A/B) = 30 ms.
10. Measure low level: limit = -2.000 V ± 7 mV.

11. Set HP 8160A HIL (A/B) = 1 V LOL (A/B) = -1 V.
12. Set HP 8160A: DEL (A/B) = 80 ms.
13. Adjust A151/R247 for high level = 1.004 V ± 3 m V.
14. Set HP 8160A: DEL (A/B) = 30 ms.
15. Measure low level: limit = -1.004 V ± 3 mV.

16. Set HP 8160A: HIL (A/B) = 2.99 V LOL (A/B) = -2.99 V.
17 Set HP 8160A: DEL (A/B) = 80 ms.
18. Adjust A151/R268 for high level = 3.008 V ± 10 mV.
19. Set HP 8160A: DEL (A/B) = 30 ms.
20. Measure low level: limit = -3.008 V ± 10 m V.

21. Set HP 8160A: HIL (A/B) = 3.99 V LOL (A/B) = -3.99 V
22. Set HP 8160A: DEL (A/B) = 80 ms.
23. Adjust A151/R266 for high level = 4.014 V ± 12 mV.
24. Set HP8160A: DEL (A/B) = 30 ms.
25. Measure low level:limit = -4.014 V ± 12 mv.

26. Set HP 8160: HIL (A/B) = 0.99 V LOL (A/B) = -0.99 V.
27. Set HP 8160A: DEL (A/B) = 80 ms.
28. Adjust A151/R212 for high level = 0.994 V ± 2 mv.
29. Set HP 8160A: DEL (A/B) = 30 ms.
30. Measure low level: limit = -0.994 V ± 2 mV.

31. Set HP 8160A: HIL (A/B) = 0.49 V LOL (A/B) = -0.49 V.
32. Set HP 8160A: DEL (A/B) = 80 ms.
33. Adjust A151/R224 for high level = 0.49 V ± 3 mV
34. Set HP 8160A: DEL (A/B) = 30 ms.
35. Measure low level: limit = -0.49 V ± 2 mV.

36 Set HP 8160A.
   a. OUTPUT MODE (A/B) = 1 k ohm.
   b. HIL (A/B) = 15.6 V LOL (A/B) = 15.4 V.

37 Set HP 8160A: DEL (A/B) = 80 ms.
38. Adjust A151/R403 for high level = 15.6 V ± 20 mV.
39. Set HP 8160A: DEL (A/B) = 30 ms.
40. Measure low level: limit = 15.4 V ± 30 mV.

41. Set HP 8160A: HIL (A/B) = -15.4 V LOL (A/B) = -15.6 V.
42. Adjust A151/R435 for low level = -15.6 V ± 20 mV.
43. Set HP 8160A: DEL (A/B) = 80 ms.
44. Measure high level: limit = -15.4 V ± 20 mV.

45. Set HP 8160A: HIL (A/B) = 5.20 V LOL (A/B) = 5.0 V.
46. Adjust A150/R14 for high level = 5.2 V ± 10 mV.
47. Set HP 8160A: DEL (A/B) = 30 ms.
48. Measure low level: limit = 5.0 V ± 10 mV.

49. Set HP 8160A: OUTPUT MODE (A/B) = 50 ohm.
50. Set HP 8160A: HIL (A/B) = 7.73 V LOL (A/B) = 7.63 V.

51. Set HP 8160A: DEL (A/B) = 80 ms.
52. Adjust A151/R401 for high level = 7.73 V ± 5 mV.

53. Set HP 8160A: DEL (A/B) = 30 ms.
54. Measure low level: limit = 7.63 V ± 5mV.

PART 4 PULSE FLATNESS ADJUSTMENT.

SET-UP:

1. Connect the HP 8160A's OUTPUT via a 50 ohm/20 dB TEE to the sampling scope's input.
2. Connect HP 8160A's TRIG OUTPUT to the sampling scope's trigger input.

ADJUSTMENT PROCEDURE:

NOTE: Steps 10-24 need only be completed if one of the measurements in steps 1-9 is out of limits.

1. Set HP 8160A.
   a. PER = 2 ms.
   b. DEL (A/B) = 0.1 ms.
   c. WID (A/B) = 1 ms.
   d. HIL (A/B) = 8 V LOL (A/B) = 0.00 V.
2. Set scope.
   a. Vertical sensitivity = 0.2 V/div.
   b. Adjust offset to position the high level of the pulse on the vertical center line of the display (sensitivity = 2%/div.).
3. The pulse flatness between 200 us and 400 us after the pulse step must be better than 0.2%.

4. Set HP 8160A.
   a. PER = 400 us
   b. DEL (A/B) = 20 us
   c. WID (A/B) = 200 us.
5. Set scope: Time base = 20 us/div.
6. The pulse flatness between 2 us and 200 us after the pulse step must be better than 0.5%.
7. Set HP 8160A.
   a. PER = 6 us
   b. DEL (A/B) = 0.5 us
   c. WID (A/B) = 3 us
8. Set scope: Time Base = 200 ns/div.
9. Pulse flatness must be better than 1%.

10. **PRESET** resistors.
    a. A151/R131 - A151/R135 fully CCW (counter clockwise).
    b. A151/R472 to mid-position (one-half).
11. Set HP 8160A.
    a. PER = 2 ms
    b. DEL (A/B) = 0.1 ms
    c. WID (A/B) = 1 ms
    d. HIL (A/B) = 8 V LOL (A/B) = 0 V.
12. Set scope: Vertical sensitivity = 0.2 V/div. (1 division = 2%)
13. Adjust A151/R131 for best flatness, < 0.2%, between 200 us and 400 us after the pulse step.

14. Set HP 8160A.
    a. PER = 400 us
    b. DEL (A/B) = 20 us
    c. WID (A/B) = 200 us.
15. Adjust A151/R132 for best flatness, < 0.4%, between 20 us and 200 us after the pulse step.
16. Adjust A151/R133 for best flatness, < 0.5 %, between 2 us and 20 us after the pulse step.
17. Set HP 8160A.
    a. PER = 20 us
    b. DEL (A/B) = 2 us
    c. WID (A/B) = 10 us.
18. Set scope: Time base = 1 us/div.
19. In OUTPUT MODE = 50 ohms, adjust A151/R472 for best flatness, < 1%.
20. In OUTPUT MODE = 1 k ohms, adjust A151/R134 for best flatness, < 1%.

21. Repeat steps 19 and 20 for best flatness.
22. Set HP 8160A.
    a. PER = 6 us
    b. DEL (A/B) = 0.5 us
    c. WID (A/B) = 3 us.
23. Adjust A151/R135 for flatness, < 1%.
24. Repeat steps 11-23 carefully for a fine adjustment.

25. Repeat procedure for A251, OPTION 020.

11. OUTPUT AMPLIFIER TRANSISTION TIME ADJUSTMENTS.

EQUIPMENT:

Sampling oscilloscope, 50 ohm/20 dB TEE.

SET-UP:

1. Set HP 8160A.
   a. PER = 100 ns
   b. DEL (A/B) = 0 ns
   c. WID (A/B) = 50 ns
   d. LEE (A/B) = 3 ns TRE (A/B) = 3 ns

2. Set scope.
   a. Horizontal Amplifier = 1 ns/division
   b. Vertical Amplifier = 1 V/division.
   c. OUTPUT MODE = NORM (NORMAL)

3. Connect the HP 8160A's OUTPUT (A/B) via a 50 ohm/20 dB TEE to the scope's Channel A input.
4. Connect the HP 8160A TRIG OUTPUT to the scope's trigger input.

ADJUSTMENT PROCEDURE:

1. Set HP 8160A: HIL (A/B) = 8.00 V LOL (A/B) = 0.00 V.
2. Adjust A151/R118 for a pulse risetime and falltime of < 6 ns (pulse preshoot, overshoot, and ringing must be <= to 5%).

   NOTE: If the risetime does not meet the limit of < 6 ns do step # 9.

3. Set HP 8160A: HIL (A/B) = 1.99 V LOL (A/B) = 0.00 V.
4. Remove the 20 dB Attenuator.
5. Switch the HP 8160a's OUTPUT MODE (A/B) from NORM to COMP and check the pulse's preshoot and overshoot. It should be <= 5%. If not, alternately adjust A151/R137 in the NORM and COMP mode until the preshoot and overshoot are within limit.

6. Set OUTPUT MODE (A/B) = NORM.
7. Replace the 20 dB Attenuator.

8. Repeat steps 1-6.

9. Set HP 8160A.
   a. RCL 0
   b. PER = 100 ns
   c. WID (A/B) = 50 ns
   d. LEE (A/B) = 3 ns TRE (A/B) = 3 ns
   e. HIL (A/B) = 1 V LOL (A/B) = -1 V
10. Adjust A140/R87 for a risetime of < 6 ns.
11. Adjust A140/R90 for a falltime of < 6 ns.
12. If rise time does not meet the limit repeat step 1.

13. Set HP 8160A.
   a. PER = 50 ns
   b. DEL (A/B) = 0 ns
   c. WID (A/B) = 10 ns.
14. Adjust A228/R239 for a pulse width of 10 ns ± 0.7 ns.

15. Repeat procedure for A251, OPTION 020.

12. TRIGGER OUTPUT PULSE WIDTH AND DELAY ADJUSTMENT.

This section consists of two parts.

1. Width Adjustment
2. Delay Adjustment

PART 1 WIDTH ADJUSTMENT.

EQUIPMENT:

Sampling oscilloscope, 50 ohm/20 dB TEE

SET-UP:

1. Set HP 8160A.
   a. PER = 100 ns
   b. DEL (A) = 0 ns
   c. WID (A) = 10 ns
   d. HIL (A) = 2 V LOL (A) = 0 V.
2. Connect the HP 8160A's TRIG OUTPUT via a 50 ohm/20 dB TEE to the scope's input.
3. Connect the HP 8160A's OUTPUT (A) to the scope's trigger input.

ADJUSTMENT PROCEDURE:

NOTE: Repeat steps 1-3, if necessary, until both period limits are met.

1. Adjust A150/R102 for 40 ns ± 4 ns.

2. Set HP 8160A: PER = 1 us.
3. Pulse width = 400 ns ± 40 ns.

4. Set HP 8160A: WID A = 99.9 ns.
5. Adjust A150/C101 for 8 ns ± 1 ns.

PART 2 DELAY ADJUSTMENT.

EQUIPMENT:

1. Sampling scope, 50 ohm/20 dB TEE.
2. Pulse Generator

SET-UP:

1. Set HP 8160A.
   a. INPUT MODE = TRIG
   b. EXT SLOPE = POS

2. Connect the HP 8160A's OUTPUT (A) via a 50 ohm/20 dB TEE to the scope's input.
3. Connect the pulse generator's trigger output to the scope's trigger input.
4. Connect the pulse generator's output to the HP 8160A's EXT INPUT.

5. Adjust the HP 8160A's trigger level.

ADJUSTMENT PROCEDURE:

1. SET REFERENCE: Align the pulse's leading-edge (50% point) with the center vertical-line of the scope's display.
2. Connect the HP 8160A's TRIG OUTPUT via a 50 ohm/20 dB TEE to the scope's input.
3. The TRIG OUTPUT delay = 0 ns ± 300 ps.
4. Change A150/C112 (factory select value, 0-10 pF) if the delay is out of limit.

13. DELAY AND WIDTH FINAL ADJUSTMENTS.

This section consists of seven parts:

1. Dual channel coincidence adjustment
2. Dual channel zero delay adjustment.
3. Single channel zero delay adjustment
4. Minimum delay adjustment
5. Minimum width adjustment
6. Long delay adjustment
7. Long width adjustment.

NOTES:
1. Omit Parts 1 and 2 when adjusting the one channel instrument.
2. Omit Part 3 when adjusting the two channel instrument.
3. Check the Slope Generator Roll-off Adjustment and Roll-off Check, Amplitude, and Offset Adjustments. It may be necessary to do these as pre-adjustments before doing the Delay and Width Adjustments.

EQUIPMENT:

1. Sampling Oscilloscope, 50 ohm/20 dB TEE
2. Pulse generator
3. Counter

PART 1 DUAL CHANNEL COINCIDENCE ADJUSTMENT.

SET-UP:

1. Set HP 8160A.
   a. PER = 100 ns
   b. WID (A/B) = 40 ns
   c. DEL (A/B) = 0 ns
   d. LEE (A/B) = 3 ns TRE (A/B) = 3 ns
   e. HIL (A/B) = 2.5 V LOL (A/B) = 0 V
   f. OUTPUT MODE (A/B) = NORM
      50 ohm

2. Set the scope's horizontal sensitivity for 0.5 ns/div.

3. PRESET the following resistors fully CW and then 1/4 turn CCW:
   a. A126/R138
   b. A226/R138
   c. A326/R138
   d. A426/R138

4. Connect the HP 8160A's OUTPUT (A) via a 50 ohm/20dB TEE to the scope's input.
5. Connect the HP 8160A's TRIG OUTPUT to the scope's trigger input.

ADJUSTMENT PROCEDURE:

1. SET REFERENCE: Align the pulse's leading-edge (50%-point) with the vertical center-line of the scope's display.
2. Connect the HP 8160A's OUTPUT (B) via a 50 ohm/20 dB TEE to the scope's input.
3. Adjust A128/R219 and/or A328/R219 for alignment of the pulse's leading edge 950% point) with the reference.

PART 2 DUAL CHANNEL ZERO DELAY ADJUSTMENT.

ADJUSTMENT PROCEDURE:

1. Connect the HP 8160A's OUTPUT (A) via a 50 ohm/20 dB TEE to the scope's input.
2. Connect the HP 8160A's OUTPUT B to the scope's external trigger.
3. SET REFERENCE: Align the pulse's leading-edge (50%-point) with the vertical center-line of the scope's display.
4. Connect the HP 8160A's TRIG OUTPUT to the scope's input.
5. Adjust A127/R112 and/or A227/R112 so the pulse's leading-edge (50%-point) leads the vertical center-line by 50 ps nominal.
   NOTE: This is to assure that a zero delay can be programmed.

PART 3 SINGLE CHANNEL ZERO DELAY ADJUSTMENT.

SET-UP:

1. PRESET A126/R138 and A226/R138 fully CW and then 1/4 turn CCW.
2. Set pulse generator.
   a. PER = 100 ns.
   b. WID (A) = 50 ns
   c. HIL (A) = 1.0 V LOL (A) = 0.0 V
3. Set HP 8160A.
   a. PER = 100 ns
   b. WID (A) = 8 ns
   c. DEL (A) = 0 ns
   d. HIL (A) = 2.8 V LOL (A) = 0.0 V
   e. INPUT MODE = TRIG
   f. EXT INPUT = 50 ohms
4. Connect the HP 8160A's TRIG OUTPUT (A) via a 50 ohm/20 dB TEE to the scope's input.
5. Connect the pulse generator's output to the HP 8160A's EXT INPUT.
6. Connect the pulse generator's trigger output to the scope's trigger input.
7. Adjust the HP 8160A trigger level.

ADJUSTMENT PROCEDURE:

1. SET REFERENCE: Align the pulse's leading-edge (50% point) with the vertical center-line of the scope's display.
2. Connect the HP 8160A's OUTPUT via the 50 ohm/20 dB TEE to the scope's input.
3. Adjust A128/R219 so the pulse's leading edge (50% point) leads the reference by 50 ps nominal.
   NOTE: This is to assure that a zero delay can be programmed.

PART 4 MINIMUM DELAY ADJUSTMENT.

SET-UP:

1. Set HP 8160A.
   a. PER = 100 ns
   b. WID (A/B) = 8 ns
   c. DEL (A/B) = 0 ns
   d. LEE (A/B) = 3 ns TRE (A/B) = 3 ns
   e. HIL (A/B) = 2.8 V LOL (A/B) = 0.0 V
   f. INPUT MODE = NORM

2. Connect HP 8160A's OUTPUT (A/B) via a 50 ohm/20 dB TEE to the scope's input.
3. Connect HP 8160A's TRIG OUTPUT to the scope's trigger input.

ADJUSTMENT PROCEDURE:

1. SET REFERENCE: Align the pulse's leading edge (50% point) with the left line of the scope's display.

2. Set the HP 8160A as follows and make the adjustment required.
   a. Set DEL (A/B) = 1 ns adjust A126/R151 for 1 ns nominal.
   b. Set DEL (A/B) = 2 ns adjust A126/R153 for 2 ns nominal.
   c. Set DEL (A/B) = 3 ns adjust A126/R155 for 3 ns nominal.
   d. Set DEL (A/B) = 4 ns adjust A126/R157 for 4 ns nominal.

3. Check the HP 8160A Del (A/B) from 0.0 ns to 0.9 ns in 0.1 ns increments.
4. Change A126/C8 (factory select value, 0-10 pF) if DEL (A/B) = 0.5 ns is out of specification.

PART 5 MINIMUM WIDTH ADJUSTMENT.

SET-UP:

NOTE: The connections and parameters are the same as in PART 4 unless otherwise specified.

1. Set HP 8160A.
   a. DEL (A/B) = 0 ns .
   b. WID (A/B) = 10 ns.
2. SET REFERENCE: Align the pulse's trailing-edge (50% point) with the left line of the scope's display.

ADJUSTMENT PROCEDURE:

1. Set HP 8160A.
   a. WID (A/B) = 10 ns
   b. WID (A/B) = 11 ns
2. Adjust A226/R151 for a 1 ns increase in the width time.
3. Check width at 10.9 ns and 11.0 ns.

4. Set HP 8160A.
   a. WID (A/B) = 10 ns
   b. WID (A/B) = 12 ns
5. Adjust A226/R153 for a 2 ns increase in the width time.
6. Check width at 11.9 ns and 12.0 ns.

7. Set HP 8160A.
   a. WID (A/B) = 10 ns
   b. WID (A/B) = 13 ns
8. Adjust A226/R155 for a 3 ns increase in the width time.
9. Check width at 12.9 ns and 13.0 ns.

10. Set HP 8160A.
    a. WID (A/B) = 10 ns
    b. WID (A/B) = 14 ns
11. Adjust A226/R157 for a 4 ns increase in the width time.
12. Check width at 13.9 and 14.0 ns.

13. Set HP 8160A: set WID (A/B) from 10 ns to 10.9 ns in 0.1 ns increments and check the results.
14. Change A226/C8 (factory select value, 0-10 pF) if WID (A/B) = 10.5 ns is out of specification.

15. Set HP 8160A: WID (A/B) = 8 ns.
16. Adjust A228/R239 or A226/R138 for 8 ns ± 0.5 ns.

17. Set HP 8160A: WID (A/B) = 20 ns.
18. Check pulse width, should be 20 ns ± 1.0 ns.
19. Check pulse delay from 15-30 ns in 5 ns increments. If the output is not stable, repeat steps 15 and 16.

20. Repeat PARTS 4 and 5 if OPTION 020 is installed.

PART 6 LONG DELAY ADJUSTMENT.

SET-UP:

1. Set HP 8160;
   a. PER = 10 ms
   b. DEL (A/B) = 1 ms
   c. WID (A/B) = 1 ms
   d. LEE (A/B) = 3 ns TRE (A/B) = 3 ns
   e. HIL (A/B) = 2.4 V LOL (A/B) = 0.0 V
   f. CHANNEL A OUTPUT MODE = NORM

2. Set counter.
   a. TI A to B
   b. Channel A/B = 50 ohm, slope +. DC, X1.
   c. Gate Time = 10 ms
   d. INPUT MODE = A sep B
   e. Channel A/B trigger levels = 50% point of pulse amplitude.

3. Connect HP 8160A TRIG OUTPUT to the counter's Channel A input.
4. Connect HP 8160A OUTPUT (A/B) to the counter's channel B input.

ADJUSTMENT PROCEDURE:

1. Counter reading = 1.00 ms ± 10 us.
2. Adjust A128/C10 for 1.00 ms ± 1 us.

PART 7 LONG WIDTH ADJUSTMENT.

SET-UP:

1. Set counter.
   a. Channel B trigger slope = NEG (-).
   b. Input Mode = COM.
2. Connect HP 8160A OUTPUT (A/B) to the counter's channel A input.

ADJUSTMENT PROCEDURE:

1. Counter reading = 1.00 ms ± 10 us.
2. Adjust A228/C10 for 1.00 ms ± 1 us.

3. Repeat PARTS 6 and 7 if OPTION 020 is installed.

3 THEORY OF OPERATION

CONTENTS

TABLES

INTRODUCTION

Instrument theory is divided into blocks of related information either at the module or circuit level.

A description of the block information and a list of the blocks follows the safety information.

SAFETY

The HP 8160A is a Safety Class 1 instrument.

It has an exposed metal chassis that is directly connected to earth potential through the line power cable.

Before servicing the instrument, review:

1. The Safety Summary, page ix (red page)
2. The Instrument Reference Manuals
3. The instrument safety markings.

WARNING

Maintenance described in the service blocks is performed with power supplied to the instrument and with protective covers removed.

Such maintenance must be performed only by trained service personnel who are aware of the hazards involved, for example, fire or electrical shock.

When maintenance can be performed without power applied, the power should be removed.

SERVICE BLOCKS

Each service block except the Block Diagram service block contains the following information:

1. Component Layout Diagram
2. Theory of Operation
3. Schematic diagrams

TABLE 1. SERVICE BLOCKS/ ASSEMBLIES.

	SERVICE BLOCK	ASSEMBLY	SCHEMATICS
1.	Block Diagrams	-	-
POWER			
2.	Switched Supply	A10, A11, A12, A13	1, 2
3.	Voltage Regulators	A18	3,4
CONTROLLER			
4.	Controller (including main Motherboard)	A2 (A1)	9, 10, 11 (6)
KEYBOARD/DISPLAY/DEVICE BUS			
5.	Keyboard and Display	A3, A4	7, 8
6.	Device Bus	-	-
PULSE GENERATOR			
7.	Repetition Rate	A23	13, 14, 15
8.	Reference Trigger	A23, A127	24
9.	Burst	A20, A23	12
10.	Time Interval	A126, A226 (A326, A426)*	16, 17
		A127, A227 (A327, A427)*	18
		A128, A228 (A328, A428)*	19, 20
11.	Slope	A140 (A240)*	21, 22, 23
12.	Shift Voltage	A150, A18	5
13.	Offset Current Source	A150, A151	29
14.	Output Amplifier Control	A150 (A250)*	25, 26
15.	Output Amplifier	A151 (A251)*	27, 28

*Assemblies in parathenses '()' are OPTION 020 Assemblies.

ASSEMBLIES

Assemblies are the printed circuit boards and mounted components.

COMPONENT LAYOUT DIAGRAMS

Component layout diagrams show the placement of components on the printed circuit board. The diagrams are identified by assembly number. The number appears in bold characters in the lower left cornor of each diagram. The diagrams are located at the beginning of the service blocks.

SCHEMATIC DIAGRAMS

The assembly schematics (circuit diagrams) are identified by a bold number appearing in the lower right cornor of each diagram. The diagrams are located at the end of each service block.

TABLE 2. ASSEMBLIES/ SCHEMATIC DIAGRAMS.

NOTE: The Assemblies in parethenses are OPTION 020 boards.

ASSEMBLY	NAME	SCHEMATIC	SERVICE BLOCK
A1	Motherboard (Main)	6	4
A2	Microprocessor	9, 10, 11	4
A3	Keyboard	7	5
A4	Display	7, 8	5
A10	Motherboard (Power Supply)	1	2
A11	Switching Regulator	1	2
A12	Rectifier	2	2
A13	Filter	1	2
A18	Regulator	3, 4, 5	3
A20	Burst	12	9
A23	Repetition Rate Generator	13, 14, 15	7
A126 (A326) A226 (A426)	Time Interval 1* Delay Width	16, 17	10
A127 (A327) A227 (A427)	Time Interval 2* Delay Width	18	10
A128 (A328) A228 (A428)	Time Interval 3* Delay Width	19, 20	10
A140 (A240)	Slope Generator	21, 22, 23	11
A150 (A250)	Output Amplifier Control	24, 25, 26	14
A151 (A251)	Output Amplifier	27, 28	15

*The four assemblies within each time interval group are identical. Thus, only one schematic is provided. The delay or width function selected by a switch.

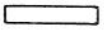
TABLE 3. SCHEMATIC DIAGRAM NOTES.

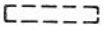
General

Units — Resistance values are in ohms, capacitance values in microfarads and inductance values in microhenries unless otherwise noted !

P/O — Part of

✳ — Asterisk denotes a factory selected value. The value shown is the nominal value.

 — Encloses front panel nomenclature.

 — Encloses rear panel nomenclature.

 — Heavy line indicates signal path.

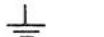
 — Heavy dashed line indicates primary feedback path.

Wire colour code. Same as resistor colour code. First number is wire body colour.

 — Wire or plug used as link.

 — Test point in a circuit. Point may/may not be identified on P.C. board.

 — Used with trimmer potentiometers or capacitors to indicate screwdriver adjustment.

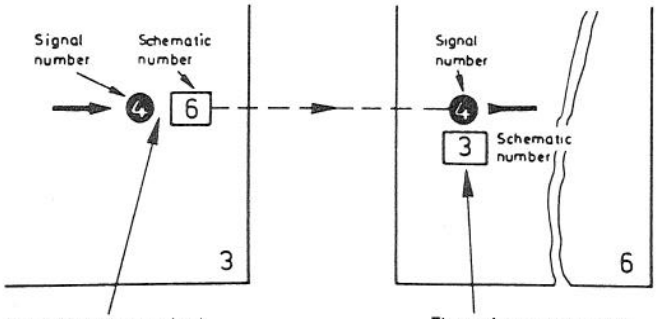
 — Direct connection to earth.

 — Ground connection to instrument chassis or frame.

 — Used when a number of common-return connections are at the same potential. If there is more than one such system in the same circuit, numbers are written in the triangles so that all connections with the same potential have the same number.

Specific potential difference with respect to a potential reference level, eg.

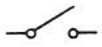
Schematic Referencing



These references on a signal leaving a schematic diagram indicate the signal destination. The circle contains the signal number and the square contains the number of the schematic to which that signal goes.

These references on a signal entering a schematic diagram indicate the signal origin. The circle contains the signal number and the square contains the number of the schematic to which that signal originates.

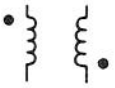
Components

 — Normally open toggle switch. Circles (O) are used for the contacts to indicate a locking type switch.

 — Spring return, 2-position transfer switch. Triangle (▲) are used for the contacts to indicate a non-locking type switch.

 — 2-position, 2-pole slide switch.

 — Air cored inductor.

 — Air cored transformer. The dot (●) is used, when necessary, to indicate instantaneous polarity.

 — Iron core

 — Ferrite core

Ferrite bead

 — Varactor diode

 — Multi-junction diode

 — Diode

 — Zener diode

 — Schottky diode

 — Light Emitting Diode (LED)

 — Photodiode

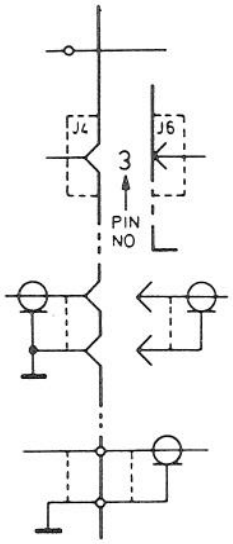
 — Fuse

 — Neon

 — Filament lamp

TABLE 3. SCHEMATIC DIAGRAM NOTES (continued).

Terminals and Connectors



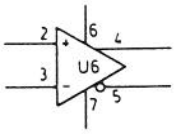
Soldered connection.

Example of fixed male and female connectors with plug and socket and contact designators, eg. P.C. board edge connector and socket.

example of bulkhead mounted coaxial socket with free coaxial plug and cable.

example of coaxial cable with termination soldered to P.C. board.

Analog Symbols



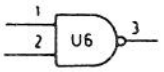
Operational amplifier

Voltage source

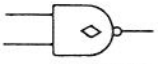
Current source

Logic Symbols

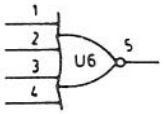
Positive logic is used unless otherwise specified.



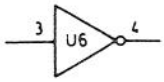
2-input NAND gate



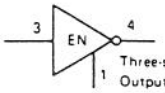
open collector



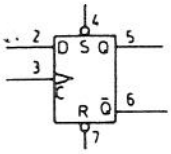
4-input NOR gate



Inverter

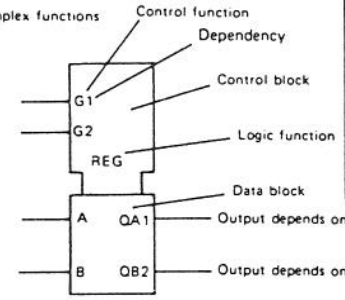


Three-state device. Output is high-impedance when EN is false, irrespective of input. Normal operation when EN is true.

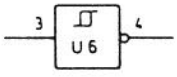


Flip-flop

Complex functions



Control functions:
G-gate, C-clock EN-3-state, R-reset (Q low) S-set (Q high), ↑ (↓) -count up (down) → shift > edge-triggered.
Logic functions:
REG-register, SEL-selector CNTR-counter, (DE)MUX-(de)multiplexer



Schmitt trigger

Wired AND connection

Wired OR connection

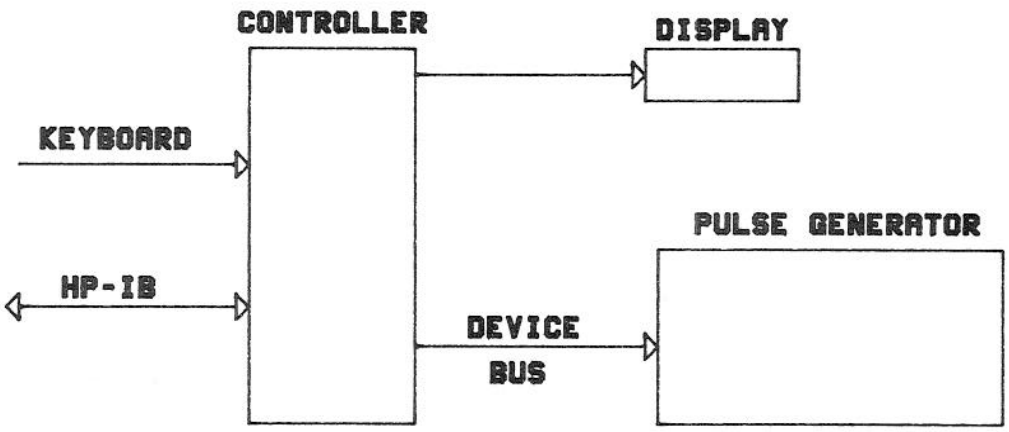
SB 1 BLOCK DIAGRAMS

CONTENTS

BLOCK DIAGRAMS

BLOCK DIAGRAMS

The following block diagram shows the major circuits of the instrument (excluding the power supply) and their relationships.



The overview of Figure 1 is expanded by the following block diagrams in this Service Block:

Figure 2. Controller and Device Bus
Figure 3. Pulse Generator
Figure 4. One Channel Board Layout (Standard Instrument)
Figure 5. Two Channel Board Layout (OPTION 020)

The figures in Service Blocks 2-15 continue this progression by providing:

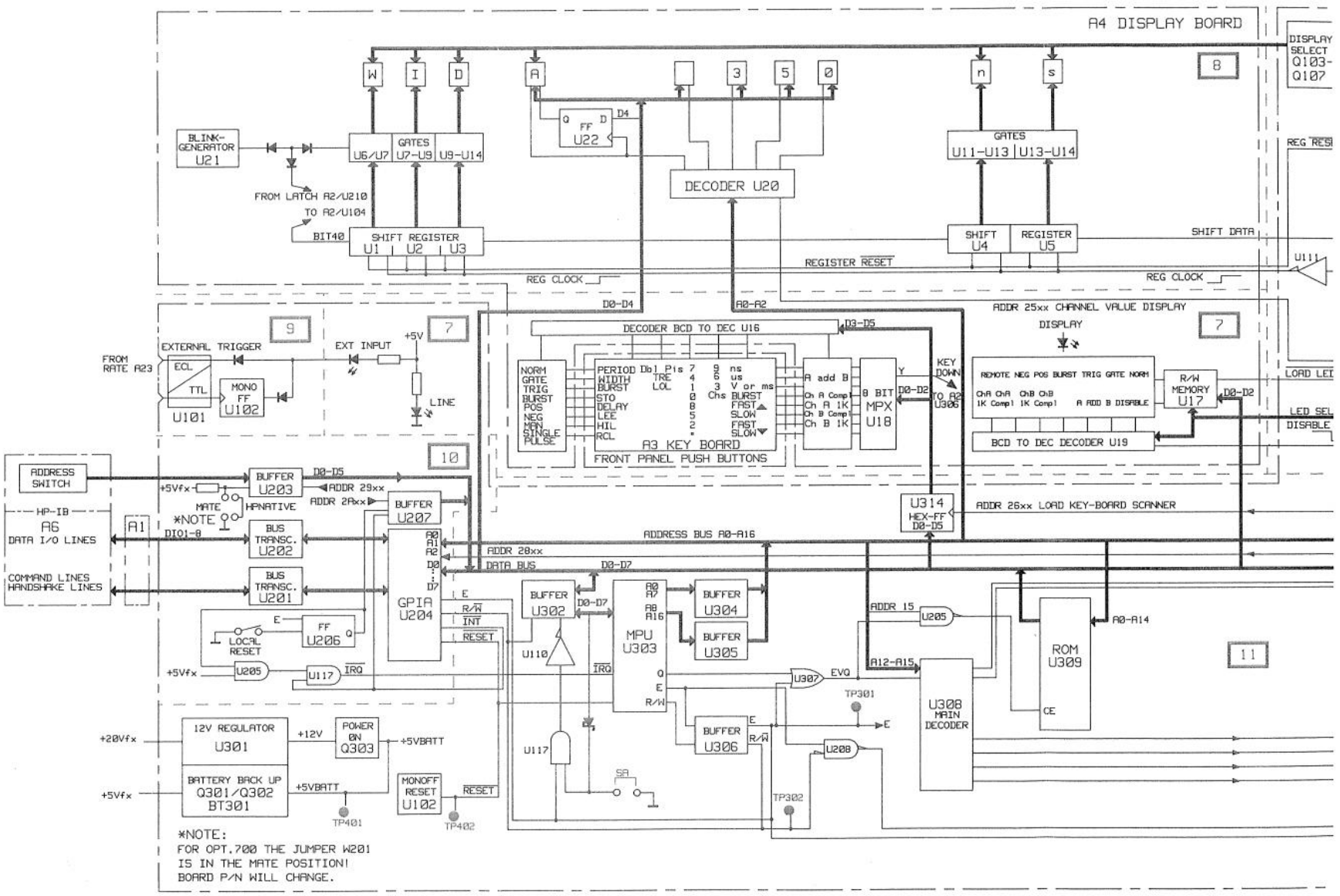
1. Component Lay-out Diagrams
2. Additional Block Diagrams
3. Schematic Diagrams.

TROUBLESHOOTING GUIDE

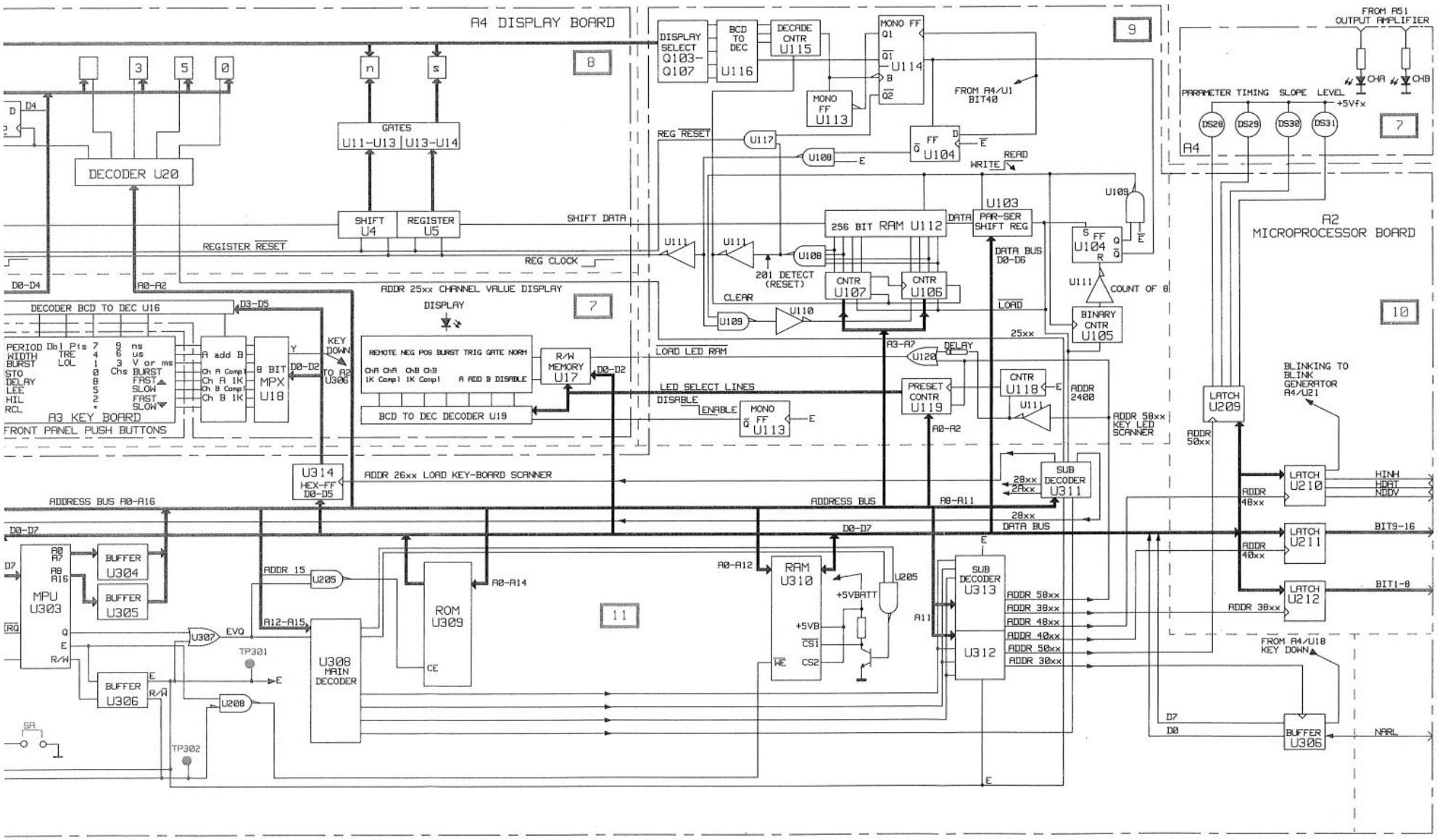
Troubleshooting is simplified by relating failures to one of the instrument major circuits.

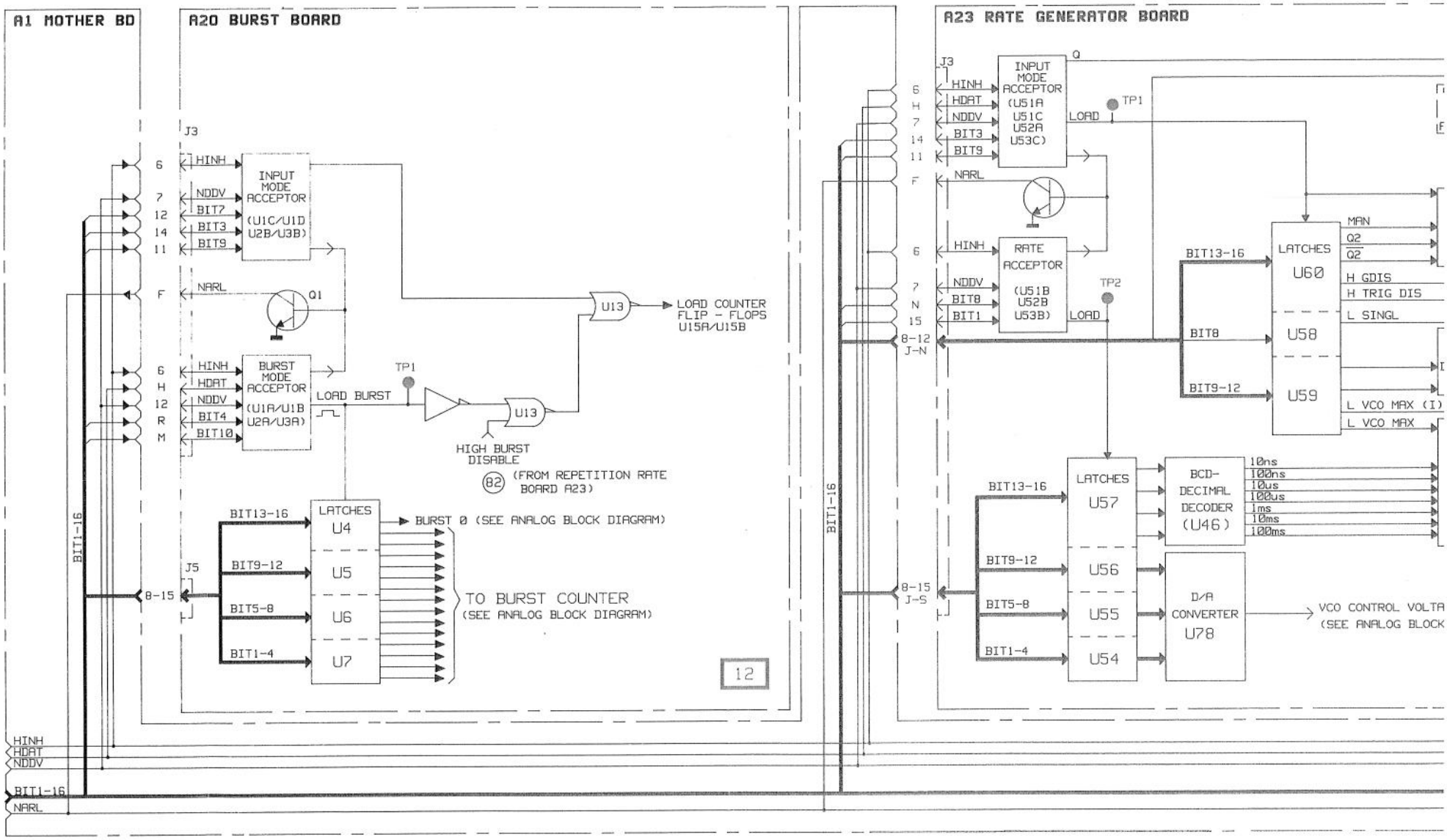
The following table lists general categories of failures and troubleshooting starting points.

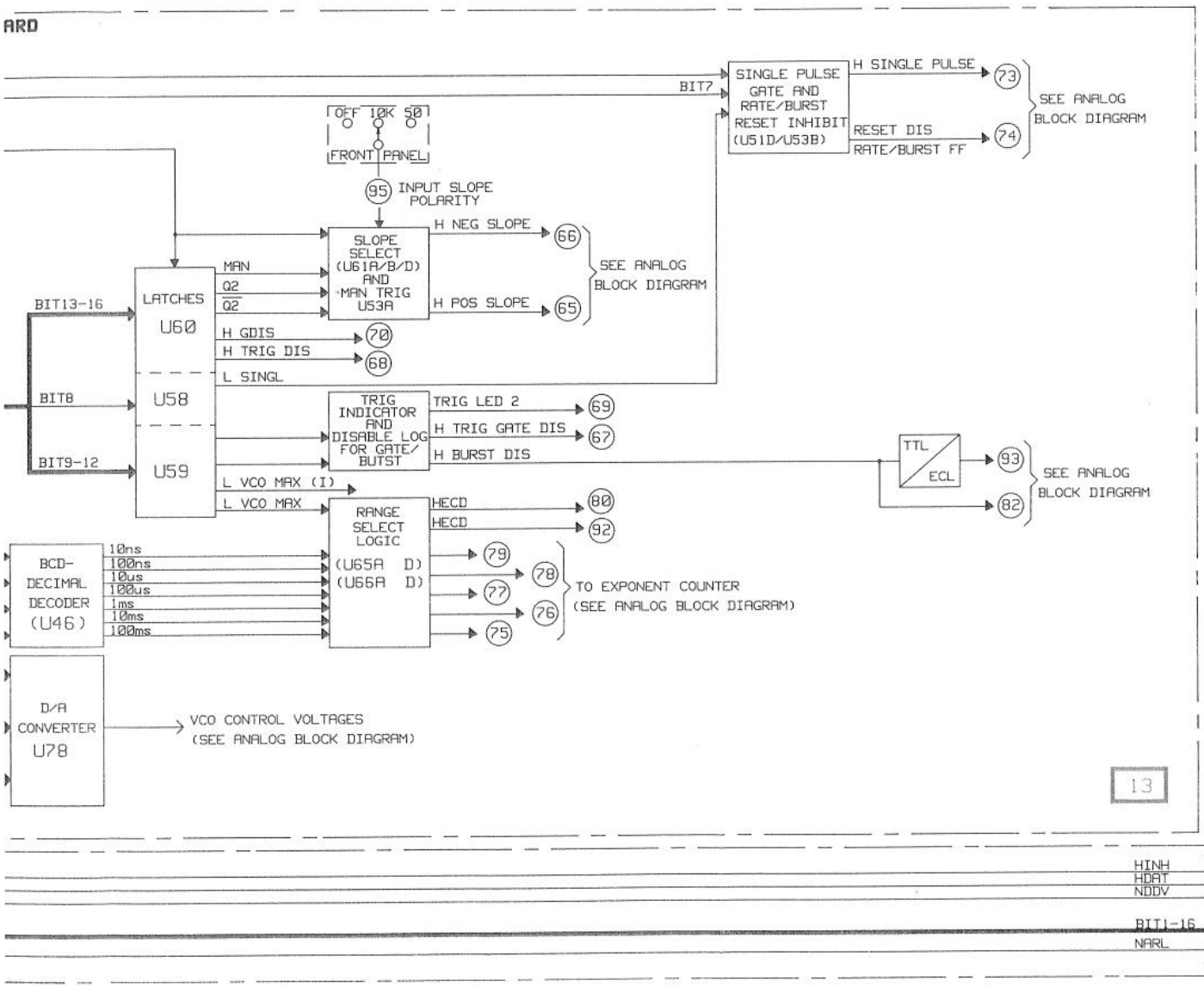
FAILURE	CIRCUIT	ASSEMBLY	SB
NO POWER-ON	Power Supply	A10-A13	2
	1. Power supply failure		
	2. Regulator board failure	A18	3
ALARM INDICATION	Another circuit attempts to overload the power supply and regulators.	A20-A151	7-15
PROGRAMMING	The failure occurs in:		
	1. Local and remote modes.	A2	4
	2. Remote mode only	A2	4
	NOTE: Check the interface cable and the controller.		
	3. Local mode only	A2, A3, A4	4, 7, 8
DISPLAY: INCORRECT	Controller	A2, 3	4,5
OUTPUT: CORRECT	Display board	A2, 4	4,5
DISPLAY: CORRECT	Device bus	A2	4
OUTPUT: INCORRECT	OUTPUT A/B and TRIG OUTPUT		
DISPLAY AND	Controller	A2	4
OUTPUT: INCORRECT	Device Bus		
TRIGGER OUTPUT: INCORRECT	TRIG OUTPUT	A23, 20	8
EXTERNAL INPUT IS INCORRECT	EXT INPUT	A23	8

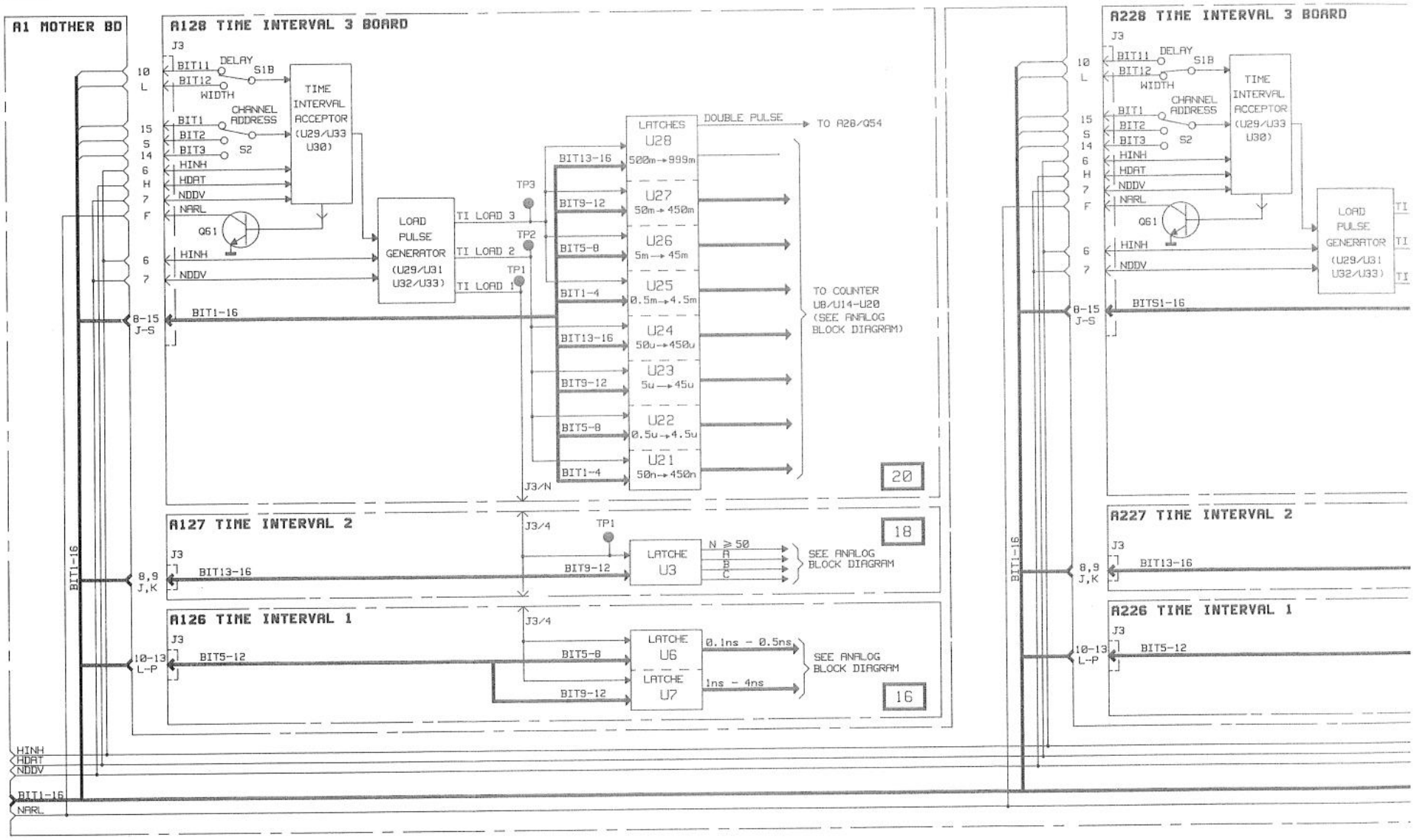


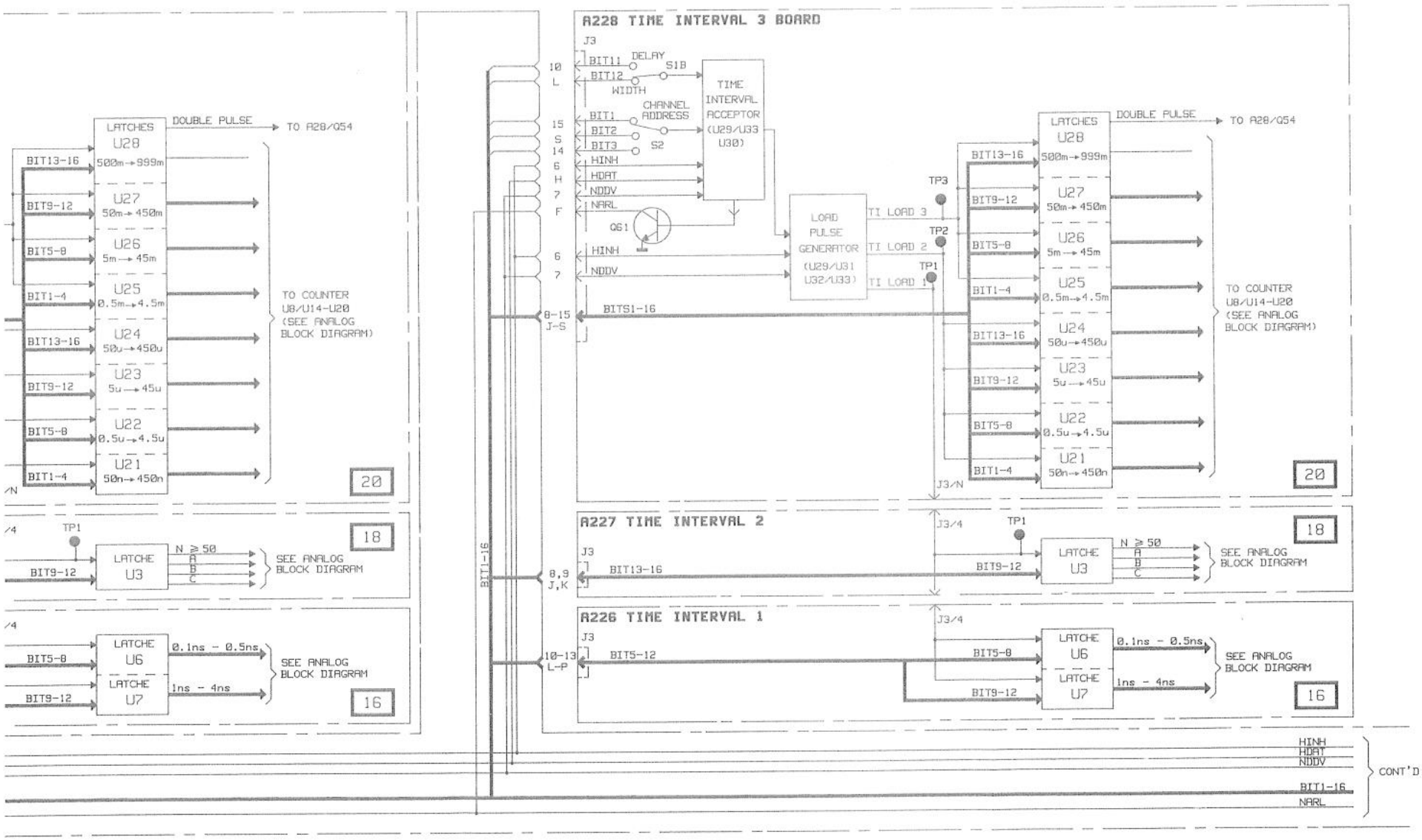
3.1-100 CONTROLLER AND DEVICE BUS (PAGE 1 OF 4)

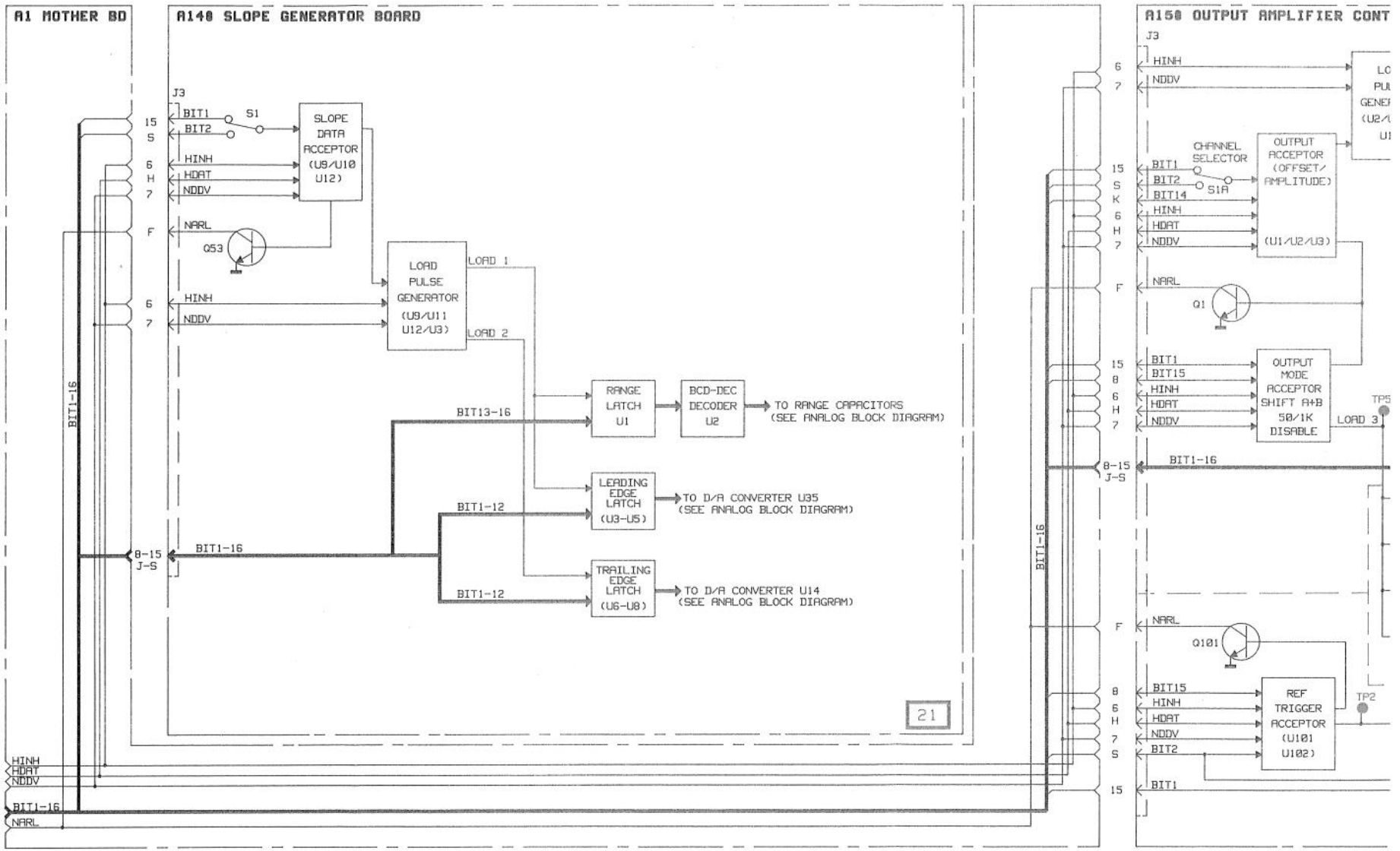

A4 DISPLAY BOARD
8
9
7
10
11
DECODER U20
GATES U11-U13 | U13-U14
SHIFT U4
REGISTER U5
SHIFT DATA
REGISTER RESET
REG CLOCK
DISPLAY SELECT Q103-Q107
BCD TO DEC U116
DECADE CNTR U115
MONO FF U113
U114
FROM A4/U1 BIT40
REG RESET
U104
READ
WRITE
256 BIT RAM U112
U103
PAR-SER SHIFT REG
DATA BUS D0-D6
201 DETECT (RESET)
CNTR U107
CNTR U106
CLEAR
LOAD
BINARY CNTR U105
COUNT OF 8
25xx
LOAD LED RAM
DELAY
U120
PRESET CONTR U119
CNTR U118
ADDR 2400
LED SELECT LINES
DISABLE
ENABLE
MONO FF U113
ADDR 50xx KEY LED SCANNER
A0-A2
A3-A7
DECODER BCD TO DEC U16
A3 KEY BOARD
FRONT PANEL PUSH BUTTONS
ADDR 25xx CHANNEL VALUE DISPLAY
DISPLAY
REMOTE NEG POS BURST TRIG GATE NORM
BCD TO DEC DECODER U19
R/W MEMORY U17
8 BIT MPX U18
A add B
KEY DOWN
TO A2 U306
U314 HEX-FF D0-D5
ADDR 26xx LOAD KEY-BOARD SCANNER
SUB DECODER U311
20xx
2Axx
ADDRESS BUS A0-A16
ADDRESS BUS
A8-A11
DATA BUS
D0-D7
MPU U303
BUFFER U304
BUFFER U305
BUFFER U306
ROM U309
A0-A14
ADDR 15
U205
A12-A15
U308 MAIN DECODER
U307
EVQ
TP301
TP302
U208
RAM U310
+5VBATT
A0-A12
A11
SUB DECODER U313
U312
ADDR 50xx
ADDR 38xx
ADDR 48xx
ADDR 40xx
ADDR 50xx
ADDR 30xx
FROM A51 OUTPUT AMPLIFIER
CHA
CHB
PARAMETER TIMING
SLOPE
LEVEL
+5Vfx
DS28
DS29
DS30
DS31
A4
A2 MICROPROCESSOR BOARD
LATCH U209
ADDR 50xx
BLINKING TO BLINK GENERATOR A4/U21
LATCH U210
LATCH U211
LATCH U212
ADDR 40xx
ADDR 30xx
HINH
HDAT
NDDV
BIT9-16
BIT1-8
FROM A4/U18 KEY DOWN
BUFFER U306
NARL

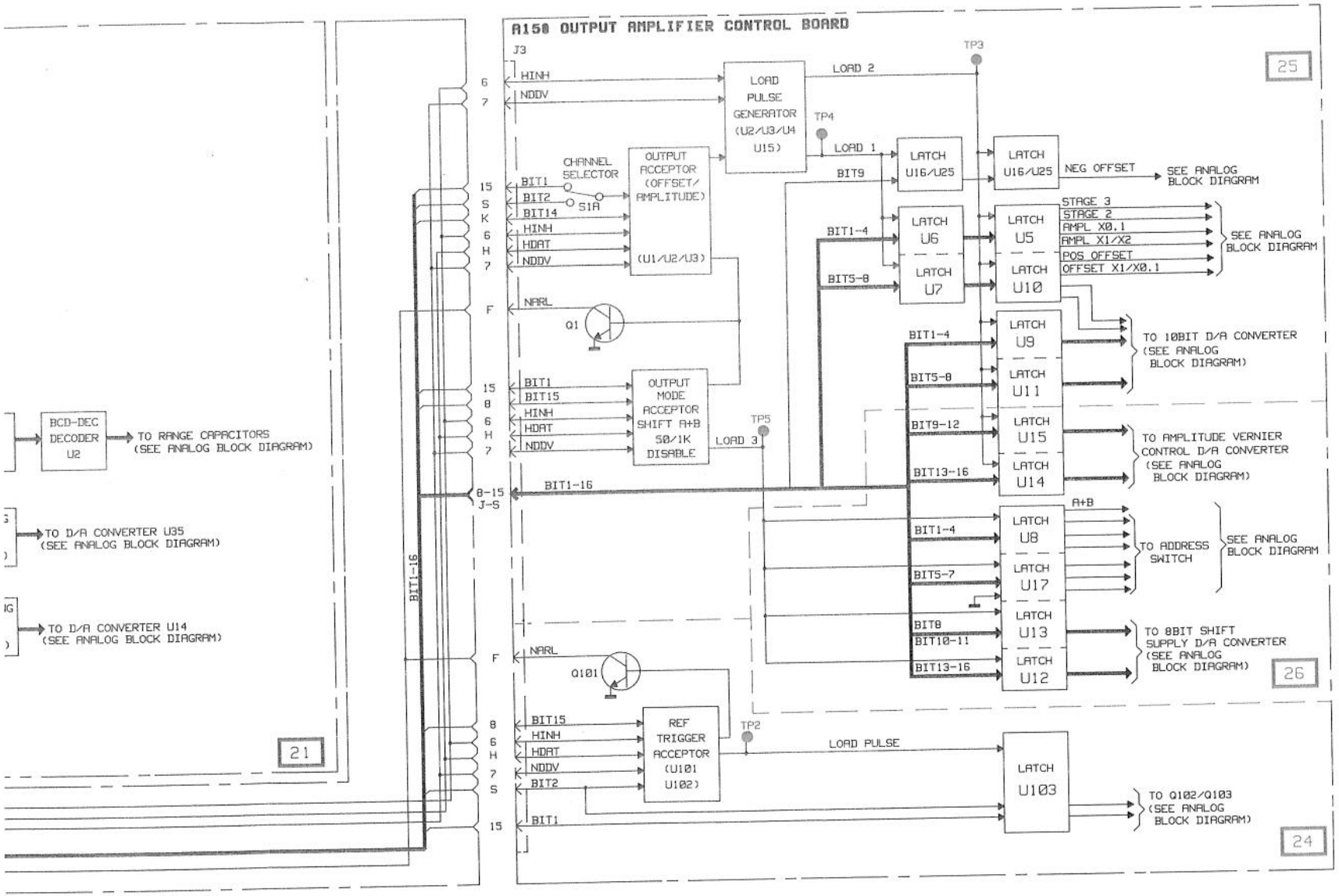

A1 MOTHER BD
A20 BURST BOARD
A23 RATE GENERATOR BOARD
J3
HINH
NDDV
BIT7
BIT3
BIT9
INPUT MODE ACCEPTOR
(U1C/U1D U2B/U3B)
NARL
Q1
U13
LOAD COUNTER FLIP - FLOPS U15A/U15B
HDAT
BIT4
BIT10
BURST MODE ACCEPTOR
(U1A/U1B U2A/U3A)
TP1
LOAD BURST
HIGH BURST DISABLE
(B2) (FROM REPETITION RATE BOARD A23)
BIT13-16
LATCHES
U4
BURST Ø (SEE ANALOG BLOCK DIAGRAM)
BIT9-12
U5
J5
8-15
BIT5-8
U6
TO BURST COUNTER
(SEE ANALOG BLOCK DIAGRAM)
BIT1-4
U7
BIT1-16
12
INPUT MODE ACCEPTOR
(U51A U51C U52A U53C)
Q
LOAD
TP1
RATE ACCEPTOR
(U51B U52B U53B)
TP2
8-12 J-N
LATCHES
U60
U58
U59
MAN
Q2
H GDIS
H TRIG DIS
L SINGL
L VCO MAX (I)
L VCO MAX
LATCHES
U57
U56
U55
U54
BCD-DECIMAL DECODER (U46)
10ns
100ns
10us
100us
1ms
10ms
100ms
D/A CONVERTER U78
VCO CONTROL VOLTA
(SEE ANALOG BLOCK
HINH
HDAT
NDDV
BIT1-16
NARL

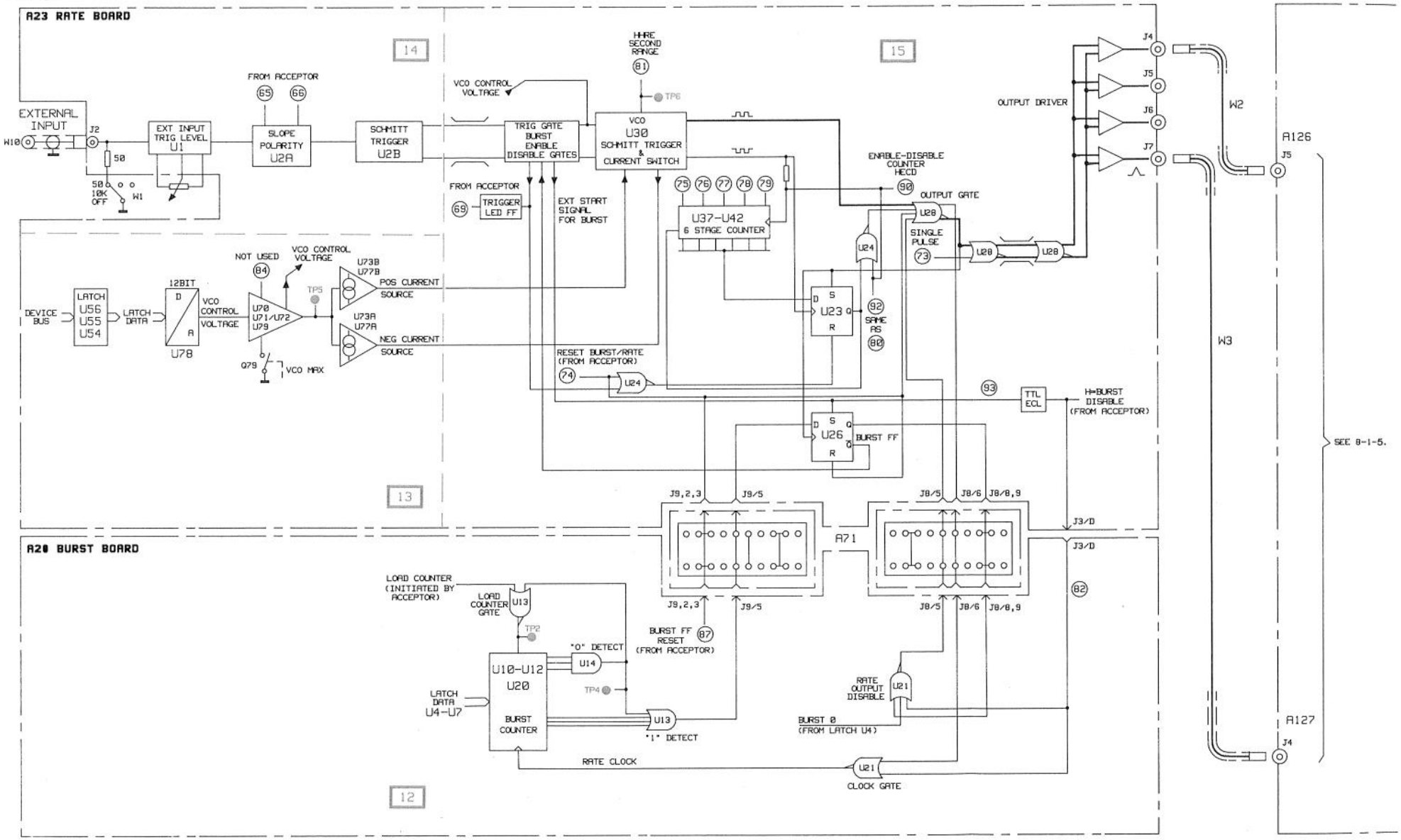

ARD
BIT7
SINGLE PULSE GATE AND RATE/BURST RESET INHIBIT (U51D/U53B)
H SINGLE PULSE
73
RESET DIS
74
RATE/BURST FF
SEE ANALOG BLOCK DIAGRAM
OFF 10K 50
FRONT PANEL
95
INPUT SLOPE POLARITY
SLOPE SELECT (U61A/B/D) AND MAN TRIG U53A
H NEG SLOPE
66
H POS SLOPE
65
SEE ANALOG BLOCK DIAGRAM
MAN
Q2
Q2
BIT13-16
LATCHES U60
H GDIS
70
H TRIG DIS
68
L SINGL
BIT8
U58
BIT9-12
U59
TRIG INDICATOR AND DISABLE LOG FOR GATE/ BUTST
TRIG LED 2
69
H TRIG GATE DIS
67
H BURST DIS
TTL
ECL
93
82
SEE ANALOG BLOCK DIAGRAM
L VCO MAX (I)
L VCO MAX
RANGE SELECT LOGIC
(U65A D)
(U66A D)
HECD
80
HECD
92
79
78
77
76
75
TO EXPONENT COUNTER
(SEE ANALOG BLOCK DIAGRAM)
BCD-DECIMAL DECODER (U46)
10ns
100ns
1us
100us
1ms
10ms
100ms
D/A CONVERTER U78
VCO CONTROL VOLTAGES
(SEE ANALOG BLOCK DIAGRAM)
13
HINH
HDAT
NDDV
BIT1-16
NARL
CONT'D


A1 MOTHER BD
A128 TIME INTERVAL 3 BOARD
J3
BIT11
BIT12
DELAY
S1B
WIDTH
BIT1
BIT2
BIT3
CHANNEL ADDRESS
S2
HINH
HDAT
NDDV
NARL
Q61
TIME INTERVAL ACCEPTOR (U29/U33 U30)
LOAD PULSE GENERATOR (U29/U31 U32/U33)
TI LOAD 3
TI LOAD 2
TI LOAD 1
TP3
TP2
TP1
LATCHES
U28
500m→999m
U27
50m→450m
U26
5m→45m
U25
0.5m→4.5m
U24
50u→450u
U23
5u→45u
U22
0.5u→4.5u
U21
50n→450n
DOUBLE PULSE
TO A28/Q54
TO COUNTER U8/U14-U20 (SEE ANALOG BLOCK DIAGRAM)
BIT1-16
BIT13-16
BIT9-12
BIT5-8
BIT1-4
J3/N
20
A127 TIME INTERVAL 2
J3/4
LATCHE U3
N ≥ 50
A
B
C
SEE ANALOG BLOCK DIAGRAM
18
A126 TIME INTERVAL 1
LATCHE U6
LATCHE U7
0.1ns - 0.5ns
1ns - 4ns
16
A228 TIME INTERVAL 3 BOARD
A227 TIME INTERVAL 2
A226 TIME INTERVAL 1
BITS1-16
HINH
HDAT
NDDV
NARL

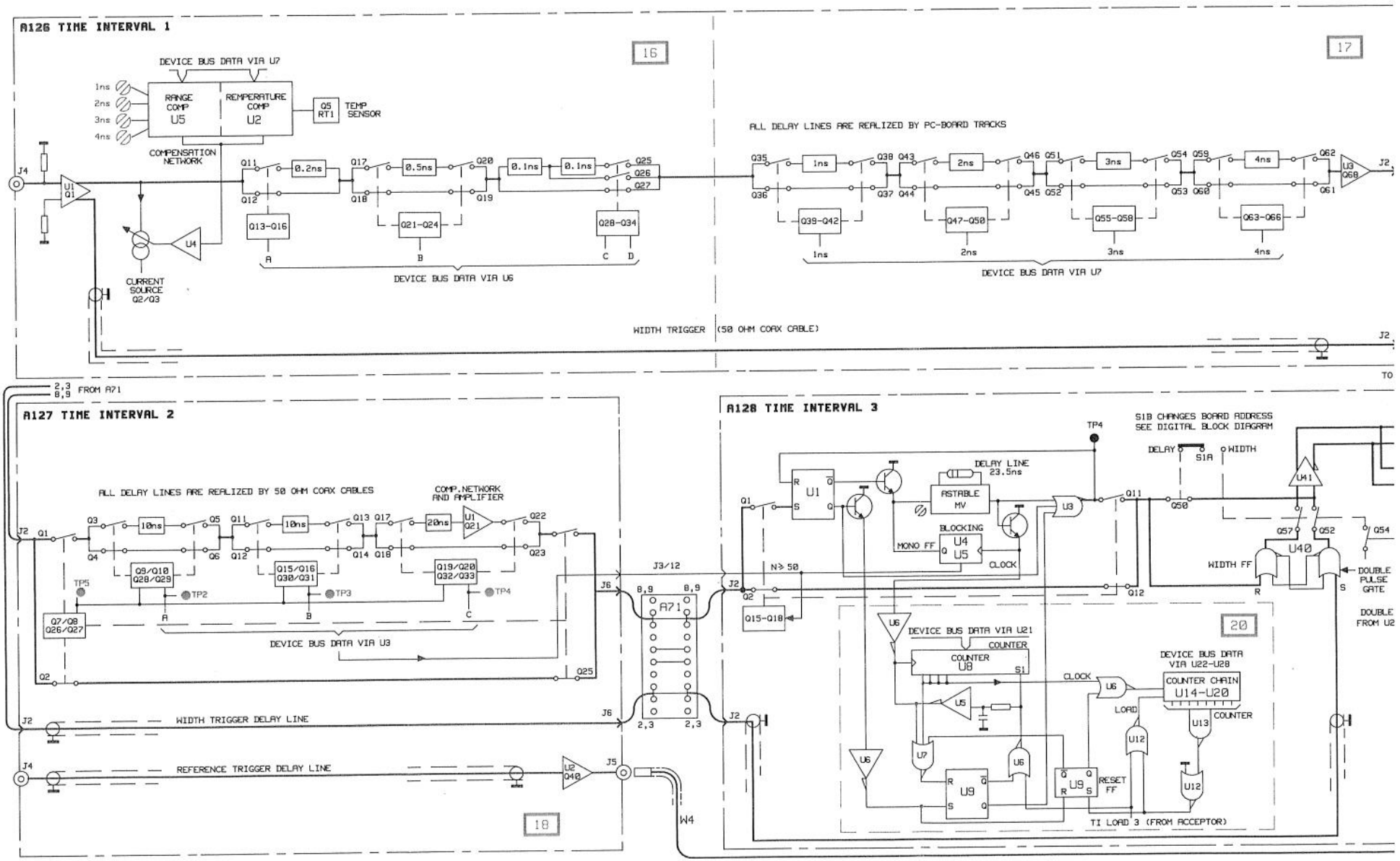

A228 TIME INTERVAL 3 BOARD
J3
BIT11
DELAY
S1B
BIT12
WIDTH
CHANNEL ADDRESS
BIT1
BIT2
BIT3
S2
HINH
HDAT
NDDV
NARL
Q61
TIME INTERVAL ACCEPTOR (U29/U33 U30)
LOAD PULSE GENERATOR (U29/U31 U32/U33)
TI LOAD 3
TI LOAD 2
TI LOAD 1
TP3
TP2
TP1
BIT1S-16
J3/N
LATCHES U28 500m→999m
U27 50m→450m
U26 5m→45m
U25 0.5m→4.5m
U24 50u→450u
U23 5u→45u
U22 0.5u→4.5u
U21 50n→450n
DOUBLE PULSE
TO A28/Q54
TO COUNTER U8/U14-U20 (SEE ANALOG BLOCK DIAGRAM)
BIT13-16
BIT9-12
BIT5-8
BIT1-4
20
A227 TIME INTERVAL 2
J3/4
LATCHE U3
N ≥ 50
A
B
C
SEE ANALOG BLOCK DIAGRAM
18
A226 TIME INTERVAL 1
LATCHE U6
LATCHE U7
0.1ns - 0.5ns
1ns - 4ns
16
HINH
HDAT
NDDV
BIT1-16
NARL
CONT'D

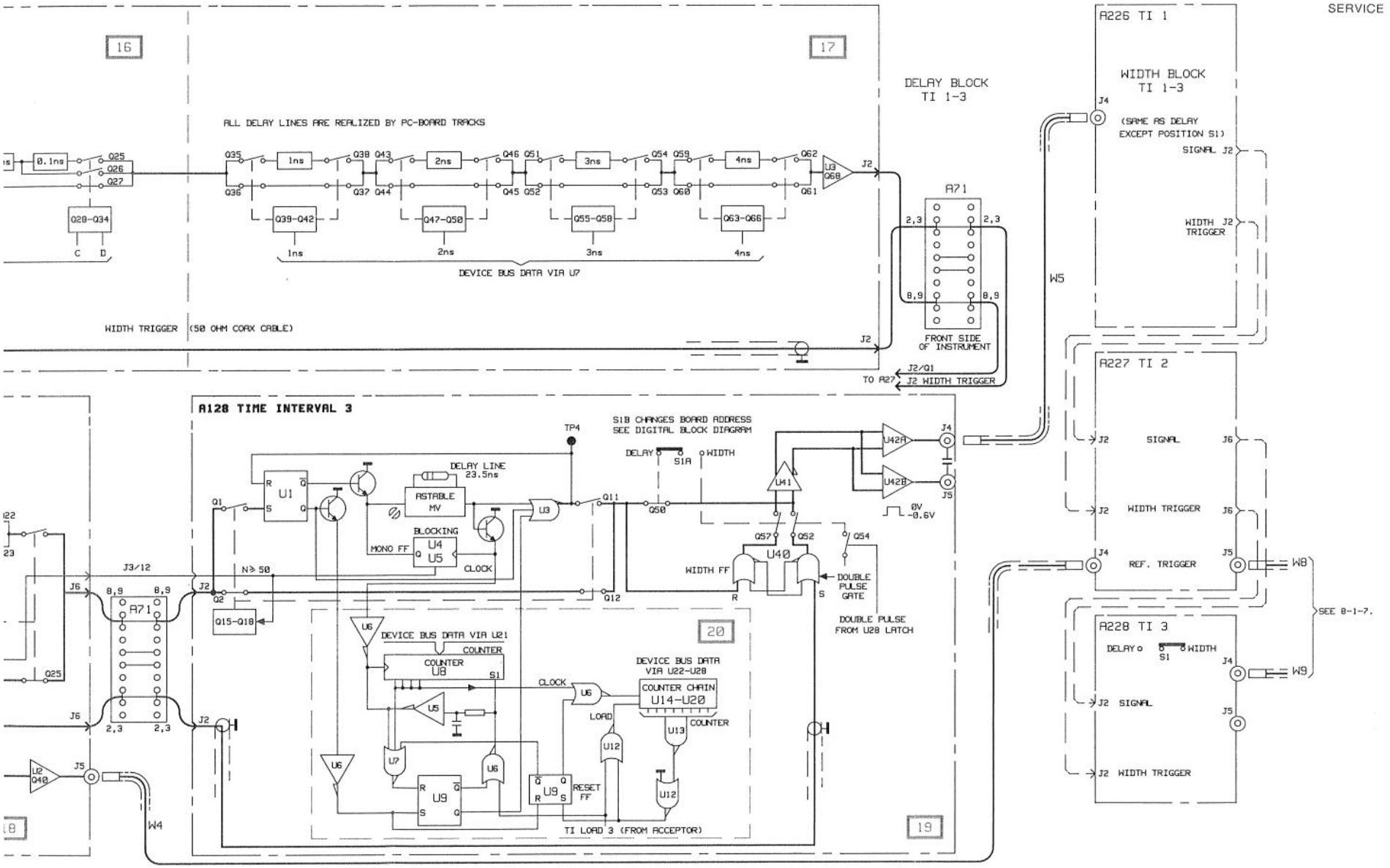

A1 MOTHER BD
A14B SLOPE GENERATOR BOARD
A15B OUTPUT AMPLIFIER CONT
J3
BIT1
BIT2
S1
SLOPE DATA ACCEPTOR (U9/U10 U12)
HINH
HDAT
NDDV
NARL
Q53
LOAD PULSE GENERATOR (U9/U11 U12/U3)
LOAD 1
LOAD 2
RANGE LATCH U1
BCD-DEC DECODER U2
TO RANGE CAPACITORS (SEE ANALOG BLOCK DIAGRAM)
BIT13-16
LEADING EDGE LATCH (U3-U5)
TO D/A CONVERTER U35 (SEE ANALOG BLOCK DIAGRAM)
BIT1-12
TRAILING EDGE LATCH (U6-U8)
TO D/A CONVERTER U14 (SEE ANALOG BLOCK DIAGRAM)
BIT1-16
8-15 J-S
CHANNEL SELECTOR
S1A
OUTPUT ACCEPTOR (OFFSET/ AMPLITUDE)
(U1/U2/U3)
Q1
BIT14
OUTPUT MODE ACCEPTOR SHIFT A+B 50/1K DISABLE
BIT15
LOAD 3
TP5
Q101
REF TRIGGER ACCEPTOR (U101 U102)
TP2
21

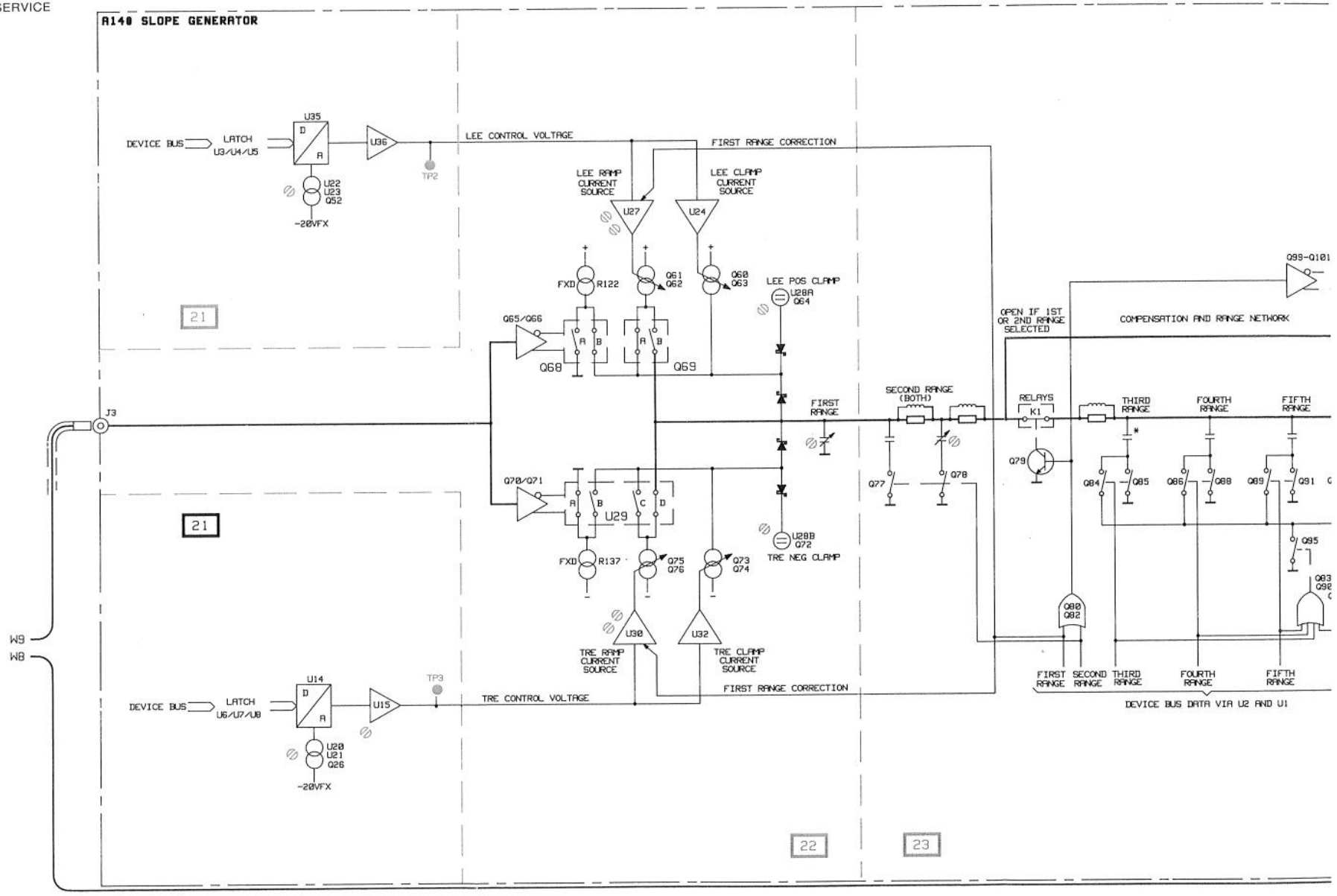

A150 OUTPUT AMPLIFIER CONTROL BOARD
J3
HINH
NDDV
LOAD PULSE GENERATOR (U2/U3/U4 U15)
LOAD 2
TP3
TP4
LOAD 1
BIT9
LATCH U16/U25
NEG OFFSET
SEE ANALOG BLOCK DIAGRAM
CHANNEL SELECTOR
S1A
BIT1
BIT2
BIT14
HDAT
OUTPUT ACCEPTOR (OFFSET/ AMPLITUDE)
(U1/U2/U3)
BIT1-4
BIT5-8
LATCH U6
LATCH U7
LATCH U5
LATCH U10
STAGE 3
STAGE 2
AMPL X0.1
AMPL X1/X2
POS OFFSET
OFFSET X1/X0.1
NARL
Q1
LATCH U9
LATCH U11
TO 10BIT D/A CONVERTER (SEE ANALOG BLOCK DIAGRAM)
BIT15
OUTPUT MODE ACCEPTOR SHIFT A+B 50/1K DISABLE
TP5
LOAD 3
BIT9-12
BIT13-16
LATCH U15
LATCH U14
TO AMPLITUDE VERNIER CONTROL D/A CONVERTER (SEE ANALOG BLOCK DIAGRAM)
BIT1-16
A+B
LATCH U8
LATCH U17
TO ADDRESS SWITCH
BIT5-7
BIT8
BIT10-11
LATCH U13
LATCH U12
TO 8BIT SHIFT SUPPLY D/A CONVERTER (SEE ANALOG BLOCK DIAGRAM)
Q101
REF TRIGGER ACCEPTOR (U101 U102)
TP2
LOAD PULSE
LATCH U103
TO Q102/Q103 (SEE ANALOG BLOCK DIAGRAM)
BCD-DEC DECODER U2
TO RANGE CAPACITORS (SEE ANALOG BLOCK DIAGRAM)
TO D/A CONVERTER U35 (SEE ANALOG BLOCK DIAGRAM)
TO D/A CONVERTER U14 (SEE ANALOG BLOCK DIAGRAM)
25
26
24
21



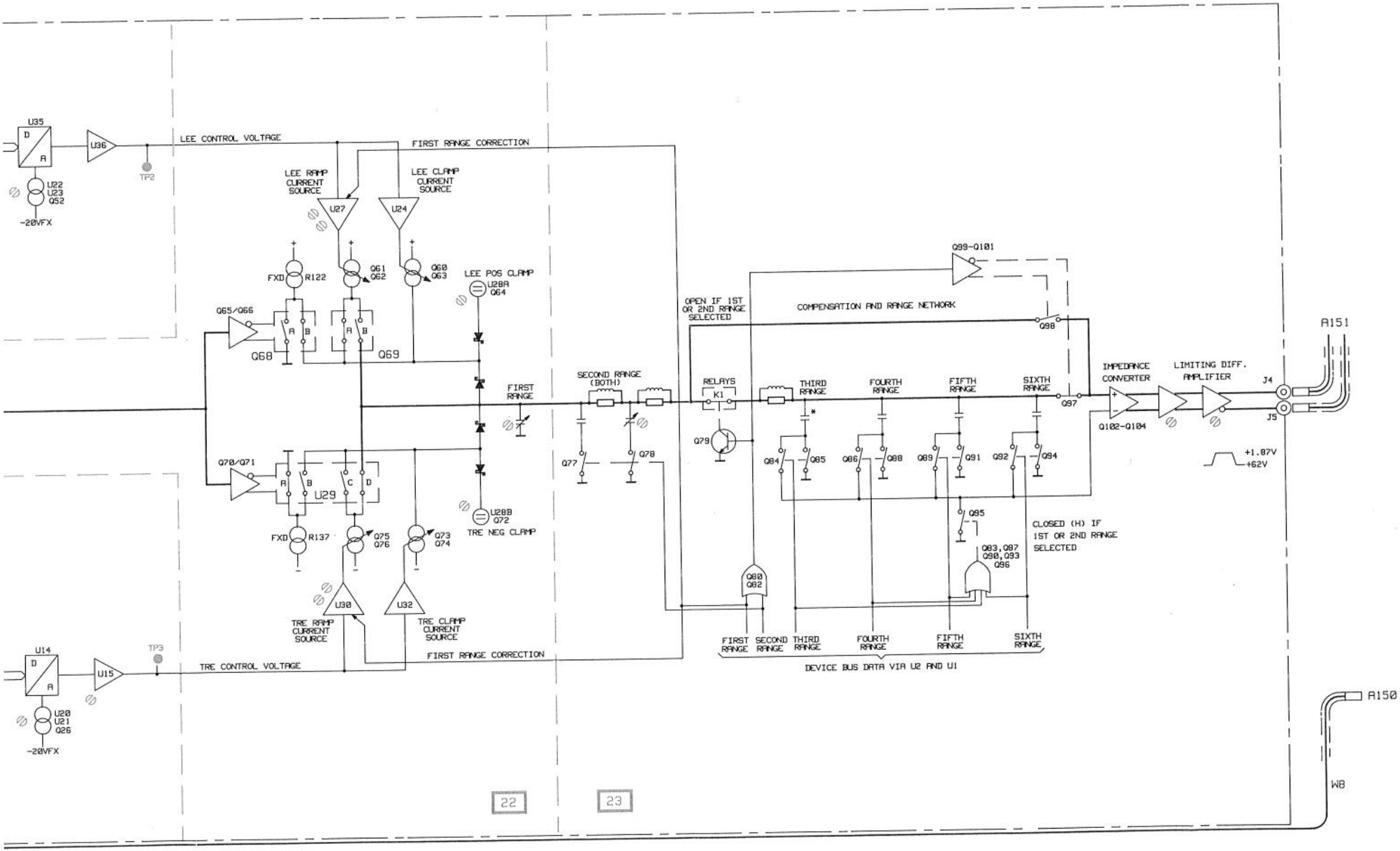
3.1-110 PULSE GENERATOR (PAGE 1 OF 4)


A126 TIME INTERVAL 1
16
17
DEVICE BUS DATA VIA U7
1ns
2ns
3ns
4ns
RANGE COMP U5
REMPERATURE COMP U2
Q5 RT1 TEMP SENSOR
COMPENSATION NETWORK
J4
U1 Q1
U4
CURRENT SOURCE Q2/Q3
Q11
0.2ns
Q17
0.5ns
Q20
0.1ns
0.1ns
Q25
Q26
Q27
Q12
Q18
Q19
Q13-Q16
Q21-Q24
Q28-Q34
A
B
C
D
DEVICE BUS DATA VIA U6
ALL DELAY LINES ARE REALIZED BY PC-BOARD TRACKS
Q35
Q36
1ns
Q38 Q43
Q37 Q44
2ns
Q46 Q51
Q45 Q52
3ns
Q54 Q59
Q53 Q60
4ns
Q62
Q61
U3 Q68
J2
Q38-Q42
Q47-Q50
Q55-Q58
Q63-Q66
1ns
2ns
3ns
4ns
DEVICE BUS DATA VIA U7
WIDTH TRIGGER (50 OHM COAX CABLE)
J2
TO
2,3 8,9 FROM A71
A127 TIME INTERVAL 2
ALL DELAY LINES ARE REALIZED BY 50 OHM COAX CABLES
COMP.NETWORK AND AMPLIFIER
J2
Q1
Q3
10ns
Q5
Q11
10ns
Q13 Q17
20ns
U1 Q21
Q22
Q4
Q6
Q12
Q14 Q18
Q23
Q9/Q10 Q28/Q29
Q15/Q16 Q30/Q31
Q19/Q20 Q32/Q33
TP5
TP2
TP3
TP4
A
B
C
Q7/Q8 Q26/Q27
DEVICE BUS DATA VIA U3
Q2
Q25
J3/12
J6
8,9
8,9
A71
2,3
2,3
J2
J6
J2
WIDTH TRIGGER DELAY LINE
J4
REFERENCE TRIGGER DELAY LINE
U2 Q40
J5
W4
18
A128 TIME INTERVAL 3
S1B CHANGES BOARD ADDRESS
SEE DIGITAL BLOCK DIAGRAM
TP4
DELAY
S1A
WIDTH
U41
DELAY LINE 23.5ns
U1
ASTABLE MV
U3
Q1
Q11
Q50
BLOCKING
MONO FF
U4 U5
CLOCK
Q57
Q52
Q54
U40
WIDTH FF
DOUBLE PULSE GATE
DOUBLE FROM U2
N≥50
Q2
Q12
Q15-Q18
20
U6
DEVICE BUS DATA VIA U21
COUNTER
COUNTER U8
S1
CLOCK
U6
DEVICE BUS DATA VIA U22-U28
COUNTER CHAIN U14-U20
U5
LOAD
U13
COUNTER
U12
U7
U6
U9
RESET FF
U12
TI LOAD 3 (FROM ACCEPTOR)

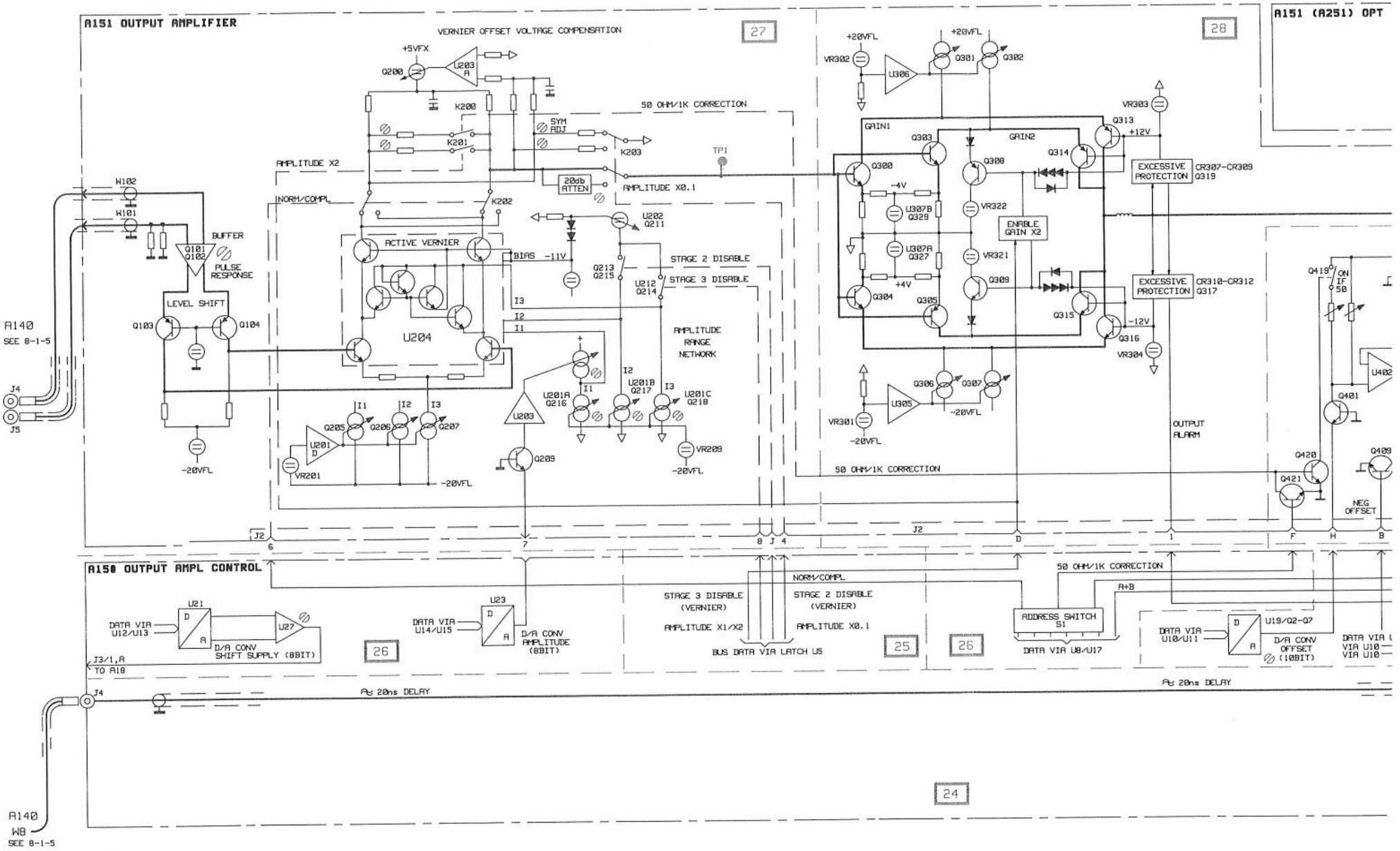

16
17
DELAY BLOCK
TI 1-3
ALL DELAY LINES ARE REALIZED BY PC-BOARD TRACKS
0.1ns
Q25
Q26
Q27
Q28-Q34
C
D
Q35
1ns
Q38 Q43
2ns
Q46 Q51
3ns
Q54 Q59
4ns
Q62
U3
Q68
Q36
Q37 Q44
Q45 Q52
Q53 Q60
Q61
Q39-Q42
Q47-Q50
Q55-Q58
Q63-Q66
1ns
2ns
3ns
4ns
DEVICE BUS DATA VIA U7
J2
WIDTH TRIGGER (50 OHM COAX CABLE)
A71
2,3
8,9
FRONT SIDE
OF INSTRUMENT
J2/Q1
TO A27
J2 WIDTH TRIGGER
A128 TIME INTERVAL 3
TP4
S1B CHANGES BOARD ADDRESS
SEE DIGITAL BLOCK DIAGRAM
DELAY
S1A
WIDTH
DELAY LINE
23.5ns
ASTABLE
MV
U1
U3
Q1
Q11
Q50
U42A
U42B
U41
J4
J5
0V
-0.6V
BLOCKING
MONO FF
U4
U5
CLOCK
Q57
Q52
Q54
U40
WIDTH FF
R
S
DOUBLE
PULSE
GATE
DOUBLE PULSE
FROM U28 LATCH
J3/12
N≥50
Q2
Q12
Q15-Q18
20
U6
DEVICE BUS DATA VIA U21
COUNTER
COUNTER
U8
S1
CLOCK
DEVICE BUS DATA
VIA U22-U28
COUNTER CHAIN
U14-U20
LOAD
U13
COUNTER
U5
U7
U9
RESET
FF
U12
TI LOAD 3 (FROM ACCEPTOR)
19
W4
W5
A226 TI 1
WIDTH BLOCK
TI 1-3
(SAME AS DELAY
EXCEPT POSITION S1)
SIGNAL J2
WIDTH J2
TRIGGER
A227 TI 2
SIGNAL
WIDTH TRIGGER
REF. TRIGGER
W8
A228 TI 3
DELAY
WIDTH
S1
SIGNAL
W9
SEE 8-1-7.

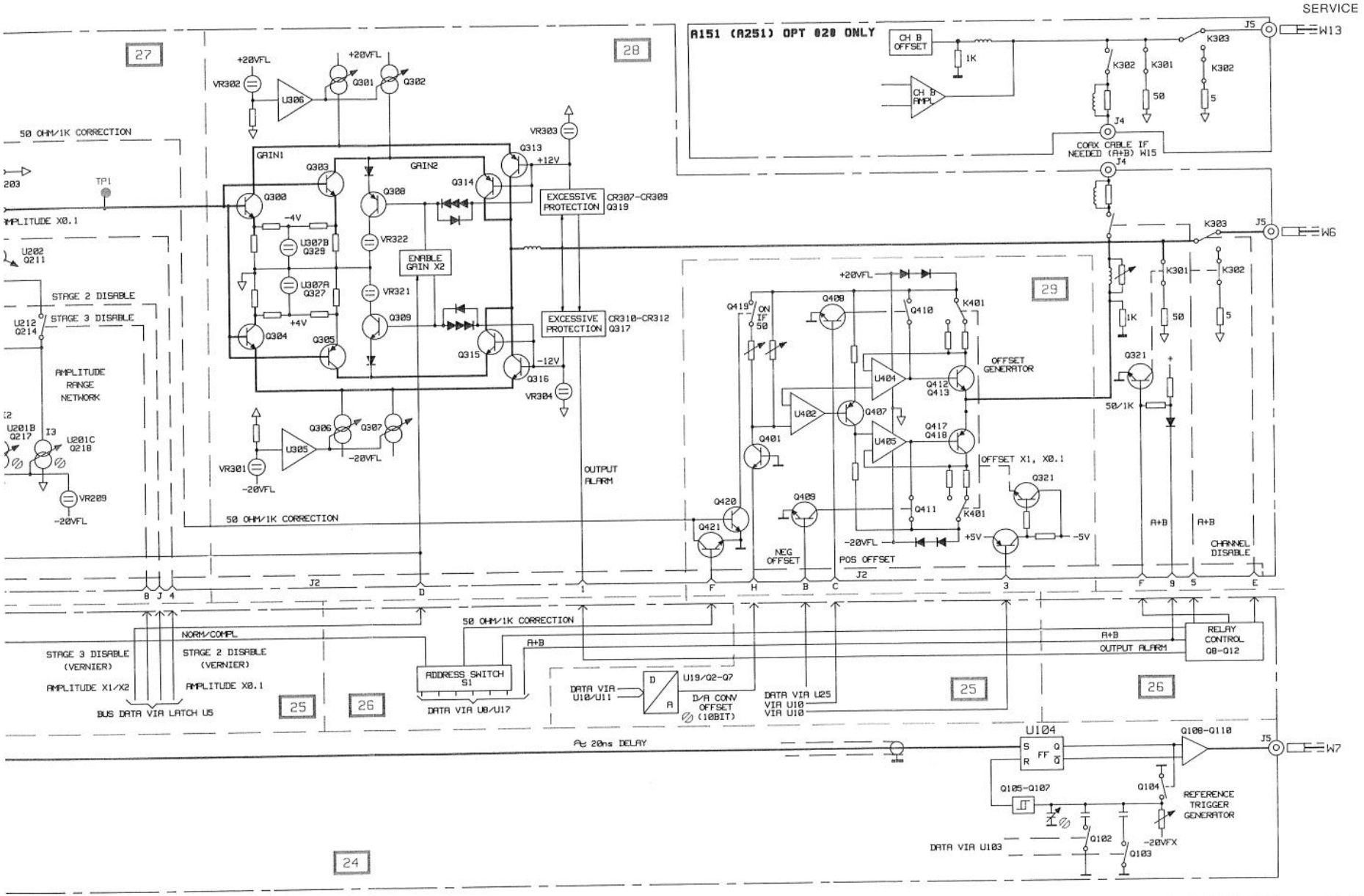


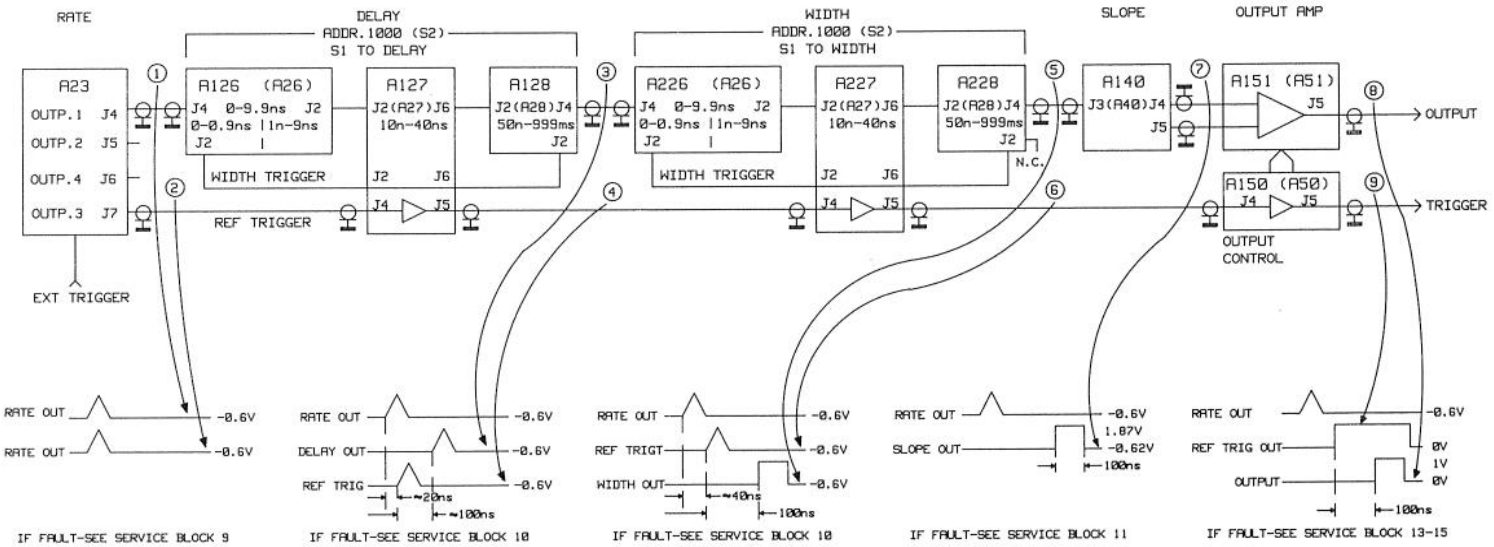
3.1-112 PULSE GENERATOR (PAGE 3 OF 4)

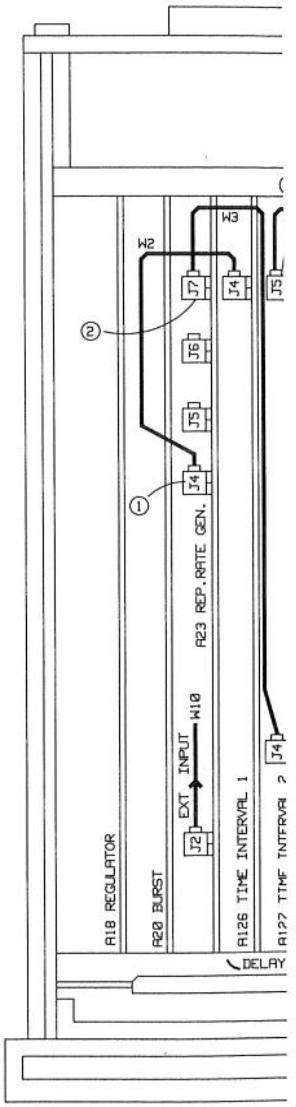

U35
D
A
U36
TP2
U22
U23
Q52
-20VFX
LEE CONTROL VOLTAGE
FIRST RANGE CORRECTION
LEE RAMP CURRENT SOURCE
LEE CLAMP CURRENT SOURCE
U27
U24
FXD
R122
Q61
Q62
Q60
Q63
LEE POS CLAMP
U28A
Q64
Q65/Q66
Q68
Q69
FIRST RANGE
SECOND RANGE (BOTH)
Q77
Q78
Q70/Q71
U29
FXD
R137
Q75
Q76
Q73
Q74
U28B
Q72
TRE NEG CLAMP
U30
U32
TRE RAMP CURRENT SOURCE
TRE CLAMP CURRENT SOURCE
U14
D
A
U15
TP3
U20
U21
Q26
-20VFX
TRE CONTROL VOLTAGE
FIRST RANGE CORRECTION
OPEN IF 1ST OR 2ND RANGE SELECTED
RELAYS
K1
Q79
Q80
Q82
Q99-Q101
COMPENSATION AND RANGE NETWORK
Q98
THIRD RANGE
FOURTH RANGE
FIFTH RANGE
SIXTH RANGE
Q97
Q84
Q85
Q86
Q88
Q89
Q91
Q92
Q94
Q95
CLOSED (H) IF 1ST OR 2ND RANGE SELECTED
Q83,Q87
Q90,Q93
Q96
IMPEDANCE CONVERTER
Q102-Q104
LIMITING DIFF. AMPLIFIER
+1.87V
+62V
J4
J5
A151
A150
W8
FIRST RANGE
SECOND RANGE
THIRD RANGE
FOURTH RANGE
FIFTH RANGE
SIXTH RANGE
DEVICE BUS DATA VIA U2 AND U1
22
23

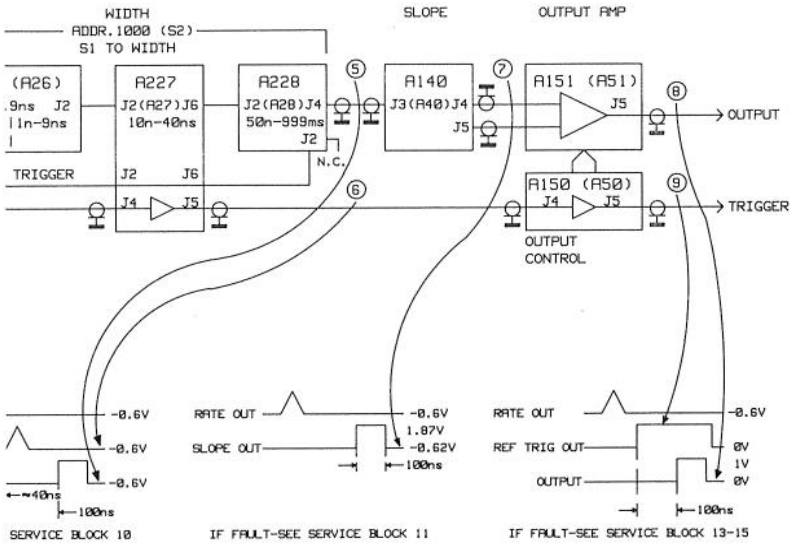
OF 4)

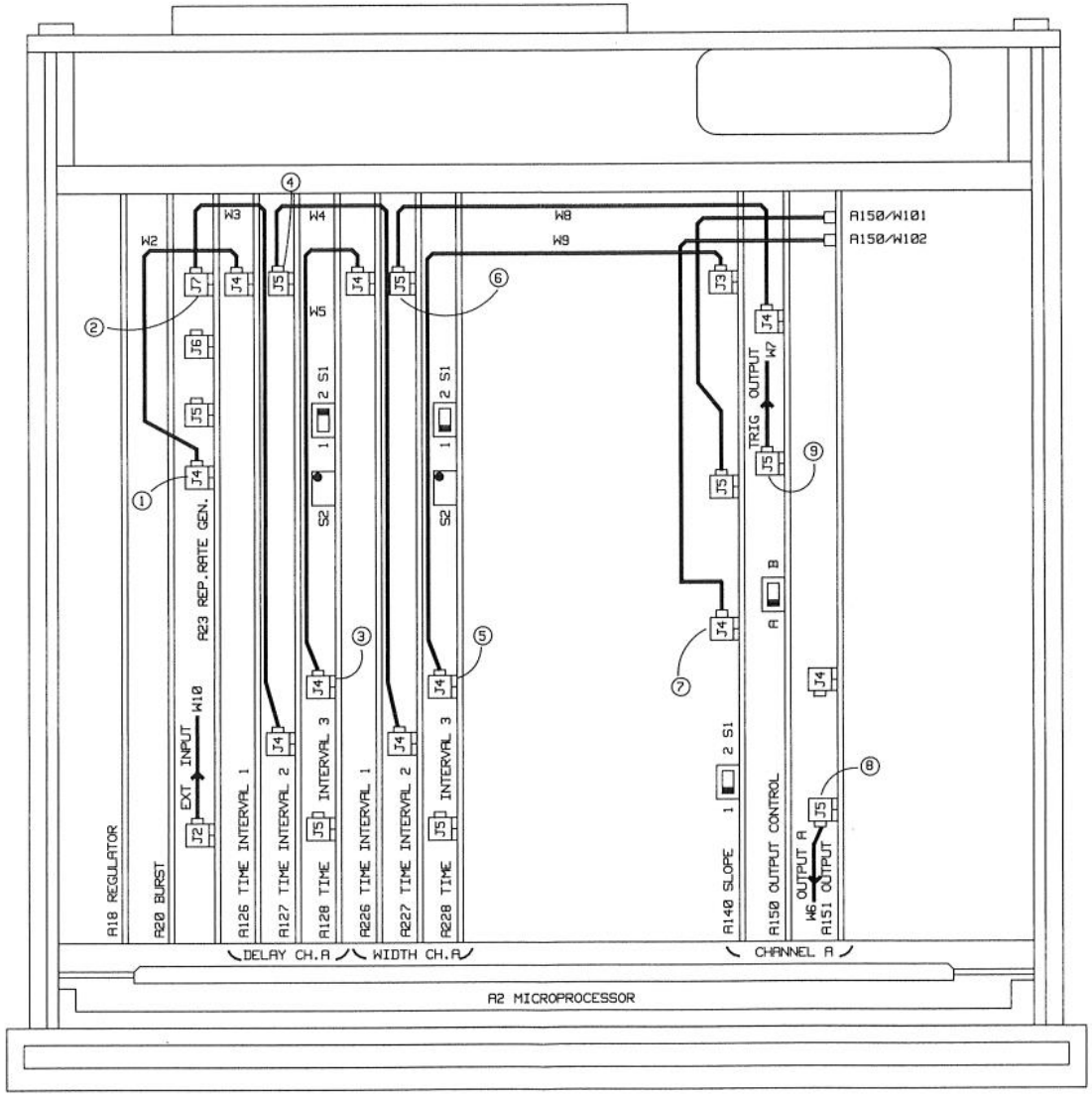

A151 OUTPUT AMPLIFIER
VERNIER OFFSET VOLTAGE COMPENSATION
27
28
A151 (A251) OPT
+5VFX
Q200
U203 A
K200
50 OHM/1K CORRECTION
SYM ADJ
K201
K203
TP1
AMPLITUDE X2
NORM/COMPL
K202
20db ATTEN
AMPLITUDE X0.1
W102
W101
BUFFER
Q101 Q102
PULSE RESPONSE
LEVEL SHIFT
Q103
Q104
A140
SEE 8-1-5
J4
J5
-20VFL
ACTIVE VERNIER
U204
BIAS -11V
U202 Q211
Q213 Q215
STAGE 2 DISABLE
U212 Q214
STAGE 3 DISABLE
I3
I2
I1
AMPLITUDE RANGE NETWORK
U201A Q216
U201B Q217
U201C Q218
U203
Q209
VR209
U201 D
Q205
Q206
Q207
VR201
+20VFL
VR302
U306
Q301
Q302
VR303
Q313
+12V
GAIN1
GAIN2
Q303
Q314
Q300
Q308
-4V
U307B Q329
VR322
ENABLE GAIN X2
U307A Q327
VR321
+4V
Q304
Q309
Q305
Q315
-12V
Q316
VR304
EXCESSIVE PROTECTION
CR307-CR309 Q319
EXCESSIVE PROTECTION
CR310-CR312 Q317
U305
Q306
Q307
VR301
-20VFL
OUTPUT ALARM
50 OHM/1K CORRECTION
Q419
ON IF 50
U402
Q401
Q420
Q421
Q409
NEG OFFSET
J2
6
7
8
J
4
D
I
F
H
B
A150 OUTPUT AMPL CONTROL
U21
DATA VIA U12/U13
D/A CONV SHIFT SUPPLY (8BIT)
U27
J3/1,A
TO A18
26
U23
DATA VIA U14/U15
D/A CONV AMPLITUDE (8BIT)
STAGE 3 DISABLE (VERNIER)
AMPLITUDE X1/X2
NORM/COMPL
STAGE 2 DISABLE (VERNIER)
AMPLITUDE X0.1
BUS DATA VIA LATCH U5
25
26
50 OHM/1K CORRECTION
A+B
ADDRESS SWITCH S1
DATA VIA U8/U17
DATA VIA U10/U11
U19/Q2-Q7
D/A CONV OFFSET (10BIT)
DATA VIA U10
VIA U10
Δ 20ns DELAY
Δ 20ns DELAY
J4
A140
W8
SEE 8-1-5
24


A151 (A251) OPT 020 ONLY
CH B OFFSET
CH B AMPL
1K
K303
K302
K301
50
5
J5
W13
J4
COAX CABLE IF NEEDED (A+B) W15
W6
27
28
29
25
26
24
50 OHM/1K CORRECTION
TP1
AMPLITUDE X0.1
+20VFL
VR302
U306
Q301
Q302
VR303
Q313
+12V
GAIN1
GAIN2
Q303
Q308
Q314
Q300
-4V
U307B Q329
VR322
ENABLE GAIN X2
U307A Q327
VR321
+4V
Q309
Q304
Q305
Q315
-12V
Q316
VR304
EXCESSIVE PROTECTION
CR307-CR309 Q319
CR310-CR312 Q317
U202 Q211
STAGE 2 DISABLE
STAGE 3 DISABLE
U212 Q214
AMPLITUDE RANGE NETWORK
U201B Q217
U201C Q218
I3
VR209
-20VFL
Q306
Q307
U305
VR301
OUTPUT ALARM
+20VFL
Q419
ON IF 50
Q408
Q410
K401
U404
Q412 Q413
OFFSET GENERATOR
U402
Q407
U405
Q417 Q418
Q401
OFFSET X1, X0.1
Q321
Q420
Q421
Q409
Q411
NEG OFFSET
POS OFFSET
+5V
-5V
50/1K
A+B
CHANNEL DISABLE
J2
B J 4
D
1
F H B C 3 F 9 5 E
NORM/COMPL
STAGE 3 DISABLE (VERNIER)
STAGE 2 DISABLE (VERNIER)
AMPLITUDE X1/X2
AMPLITUDE X0.1
BUS DATA VIA LATCH U5
ADDRESS SWITCH S1
DATA VIA U8/U17
DATA VIA U10/U11
D
A
U19/Q2-Q7
D/A CONV OFFSET (10BIT)
DATA VIA U25 VIA U10 VIA U10
RELAY CONTROL Q8-Q12
OUTPUT ALARM
20ns DELAY
U104
S
R
FF
Q
Q̄
Q108-Q110
Q105-Q107
Q104
REFERENCE TRIGGER GENERATOR
DATA VIA U103
Q102
Q103
-20VFX

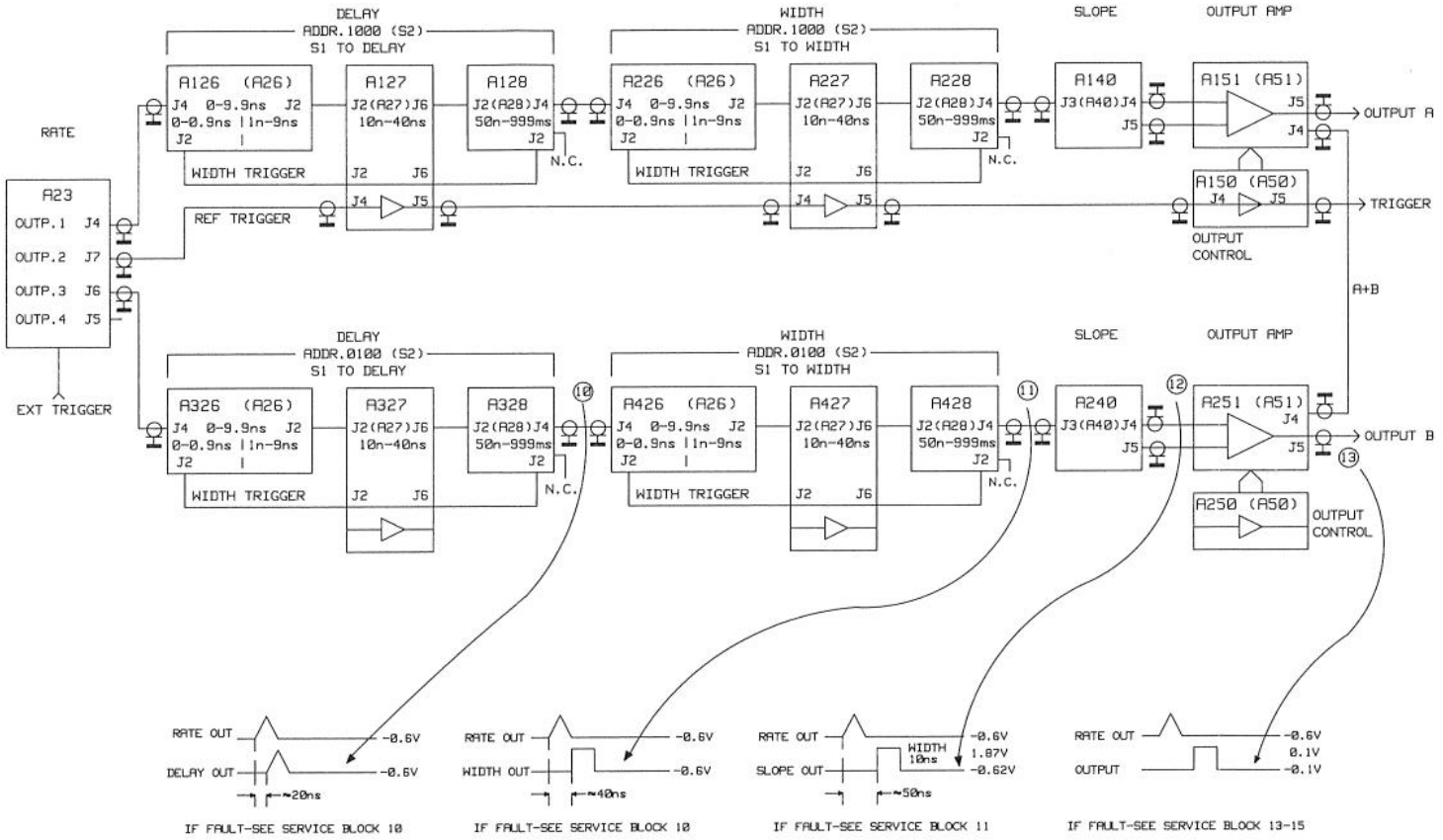

RATE
DELAY
ADDR.1000 (S2)
S1 TO DELAY
WIDTH
ADDR.1000 (S2)
S1 TO WIDTH
SLOPE
OUTPUT AMP
A23
OUTP.1 J4
OUTP.2 J5
OUTP.4 J6
OUTP.3 J7
EXT TRIGGER
A126 (A26)
J4 0-9.9ns J2
0-0.9ns ln-9ns
J2
A127
J2(A27)J6
10n-40ns
A128
J2(A28)J4
50n-999ms
J2
WIDTH TRIGGER
J2 J6
REF TRIGGER
J4 J5
A226 (A26)
J4 0-9.9ns J2
0-0.9ns ln-9ns
J2
A227
J2(A27)J6
10n-40ns
A228
J2(A28)J4
50n-999ms
J2
N.C.
A140
J3(A40)J4
J5
A151 (A51)
J5
OUTPUT
A150 (A50)
J4 J5
TRIGGER
OUTPUT
CONTROL
RATE OUT -0.6V
RATE OUT -0.6V
IF FAULT-SEE SERVICE BLOCK 9
RATE OUT -0.6V
DELAY OUT -0.6V
REF TRIG -0.6V
≈20ns
≈100ns
IF FAULT-SEE SERVICE BLOCK 10
RATE OUT -0.6V
REF TRIGT -0.6V
WIDTH OUT -0.6V
≈40ns
100ns
IF FAULT-SEE SERVICE BLOCK 10
RATE OUT -0.6V
SLOPE OUT 1.87V
-0.62V
100ns
IF FAULT-SEE SERVICE BLOCK 11
RATE OUT -0.6V
REF TRIG OUT 0V
1V
OUTPUT 0V
100ns
IF FAULT-SEE SERVICE BLOCK 13-15

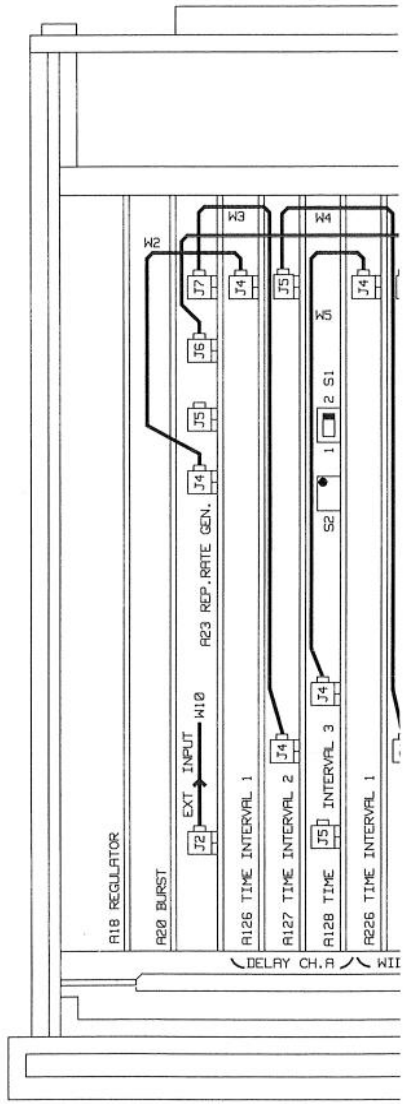

W2
W3
J7
J4
J5
J6
J5
J4
J2
EXT INPUT
W10
J4
A18 REGULATOR
A20 BURST
A23 REP.RATE GEN.
A126 TIME INTERVAL 1
A127 TIME INTERVAL 2
DELAY


WIDTH
ADDR.1000 (S2)
S1 TO WIDTH
SLOPE
OUTPUT AMP
(A26)
.9ns J2
1n-9ns
A227
J2(A27)J6
10n-40ns
A228
J2(A28)J4
50n-999ms
J2
N.C.
A140
J3(A40)J4
J5
A151 (A51)
J5
OUTPUT
TRIGGER
J2
J6
J4
J5
A150 (A50)
J4
J5
TRIGGER
OUTPUT
CONTROL
-0.6V
-0.6V
-0.6V
≈40ns
100ns
SERVICE BLOCK 10
RATE OUT
-0.6V
1.87V
SLOPE OUT
-0.62V
100ns
IF FAULT-SEE SERVICE BLOCK 11
RATE OUT
-0.6V
REF TRIG OUT
0V
1V
OUTPUT
0V
100ns
IF FAULT-SEE SERVICE BLOCK 13-15

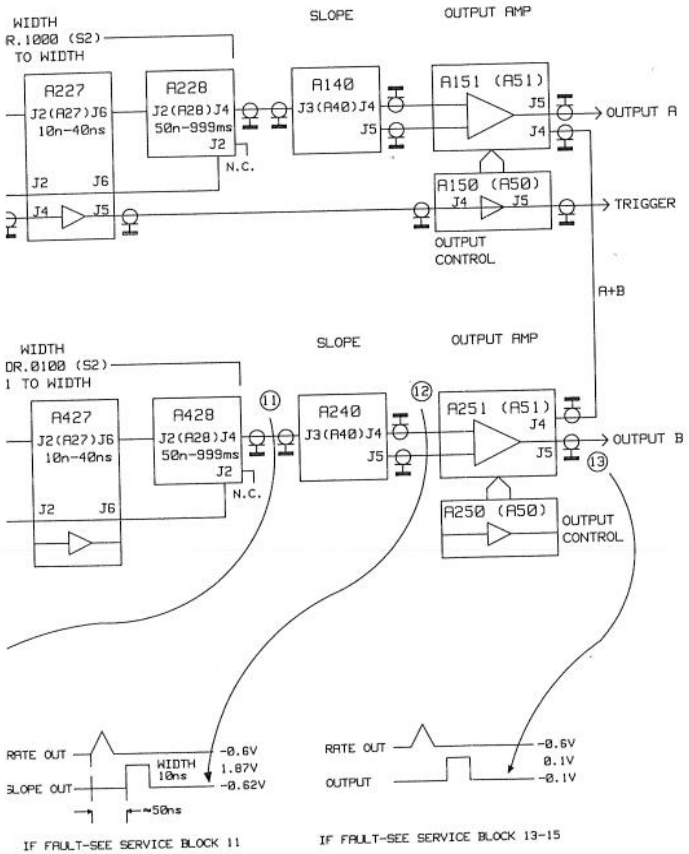

A150/W101
A150/W102
W2
W3
W4
W5
W8
W9
W10
A18 REGULATOR
A20 BURST
A23 REP.RATE GEN.
EXT INPUT
A126 TIME INTERVAL 1
A127 TIME INTERVAL 2
A128 TIME INTERVAL 3
A226 TIME INTERVAL 1
A227 TIME INTERVAL 2
A228 TIME INTERVAL 3
A140 SLOPE
A150 OUTPUT CONTROL
TRIG OUTPUT
W7
OUTPUT A
W6
A151 OUTPUT
DELAY CH.A
WIDTH CH.A
CHANNEL A
A2 MICROPROCESSOR

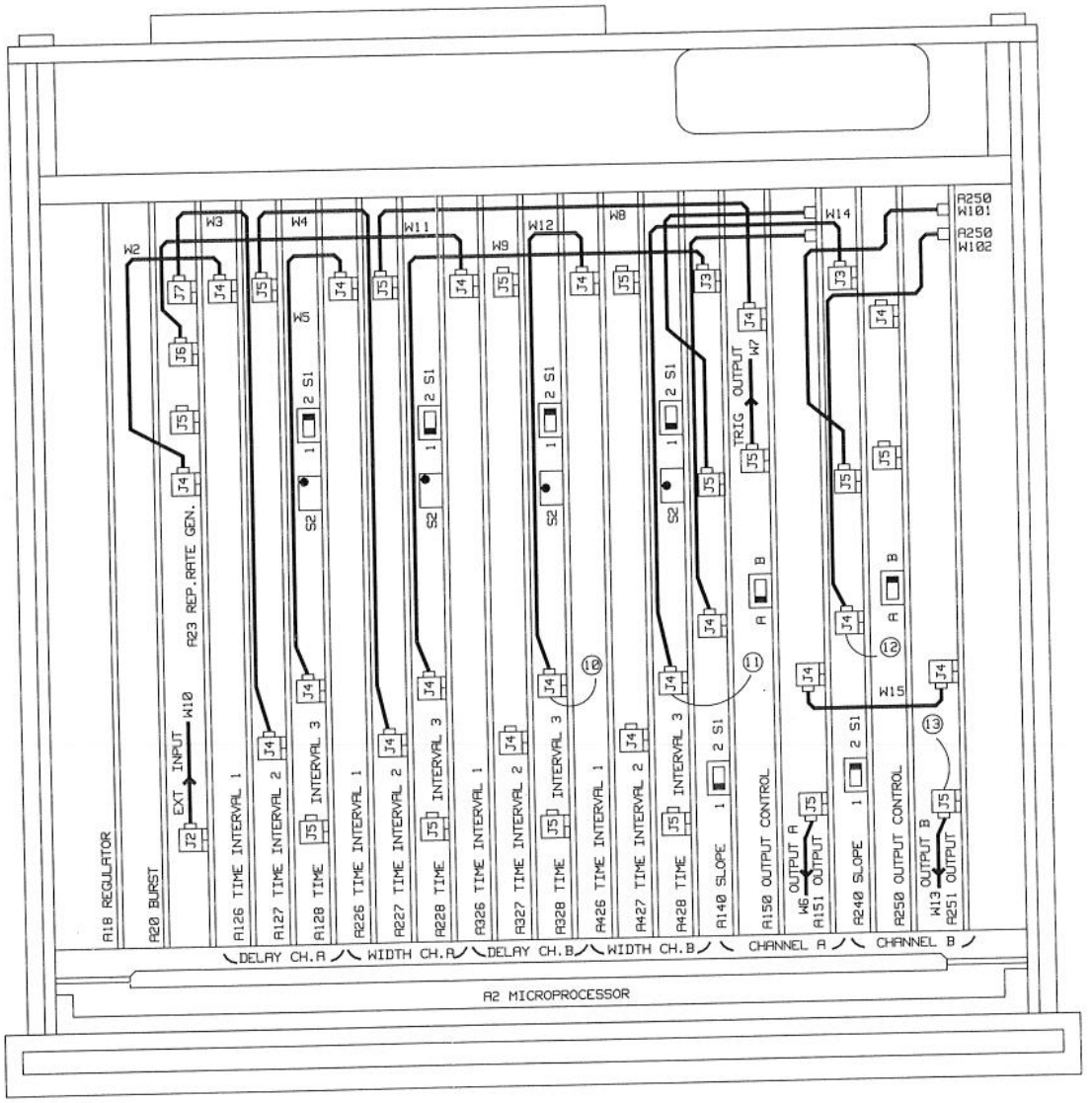
8160A OPT. 020 BLOCKDIAGRAM (TWO CHANNEL)





RAM (TWO CHANNEL)





SB 2 POWER SUPPLY

CONTENTS

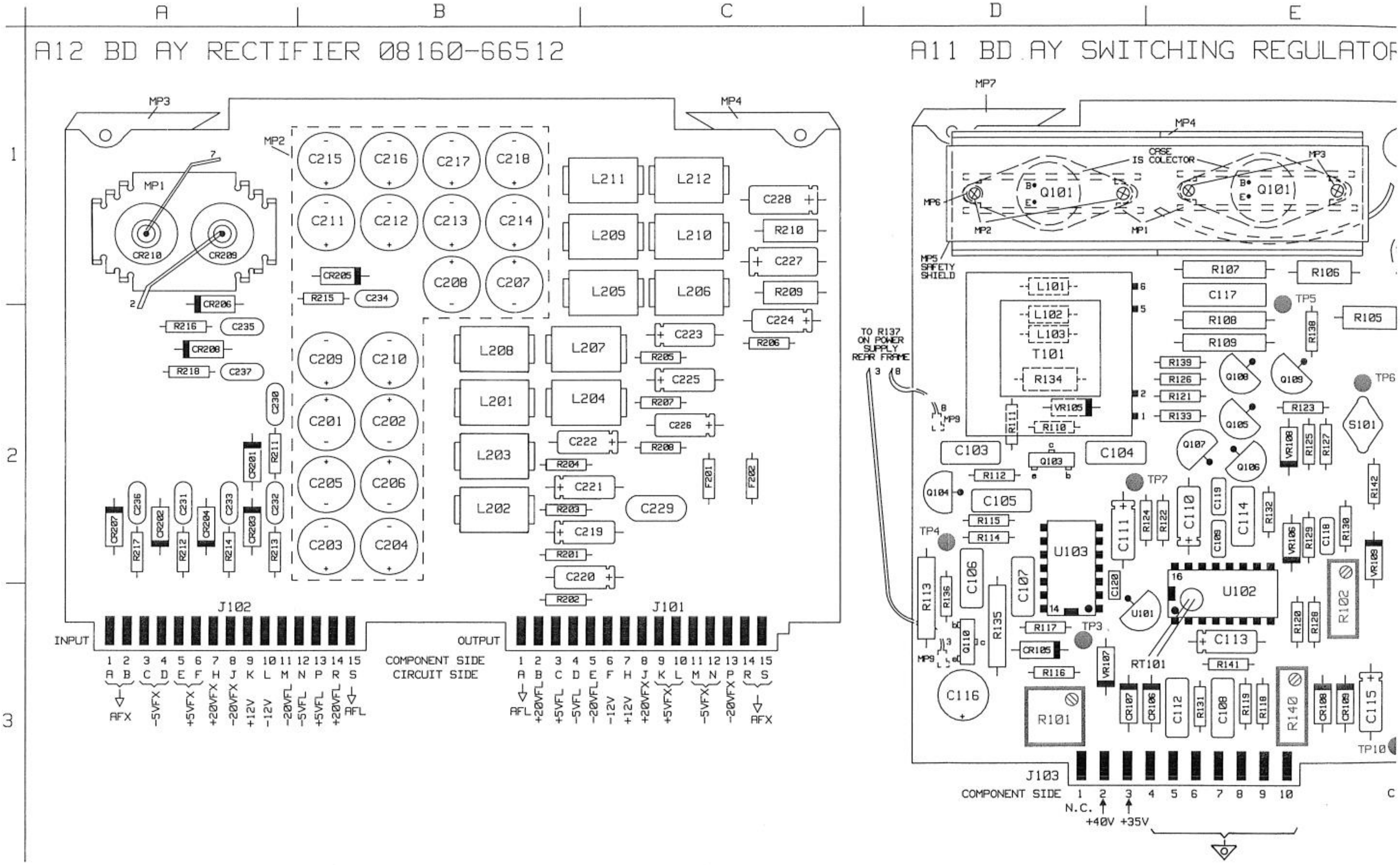
ASSEMBLIES

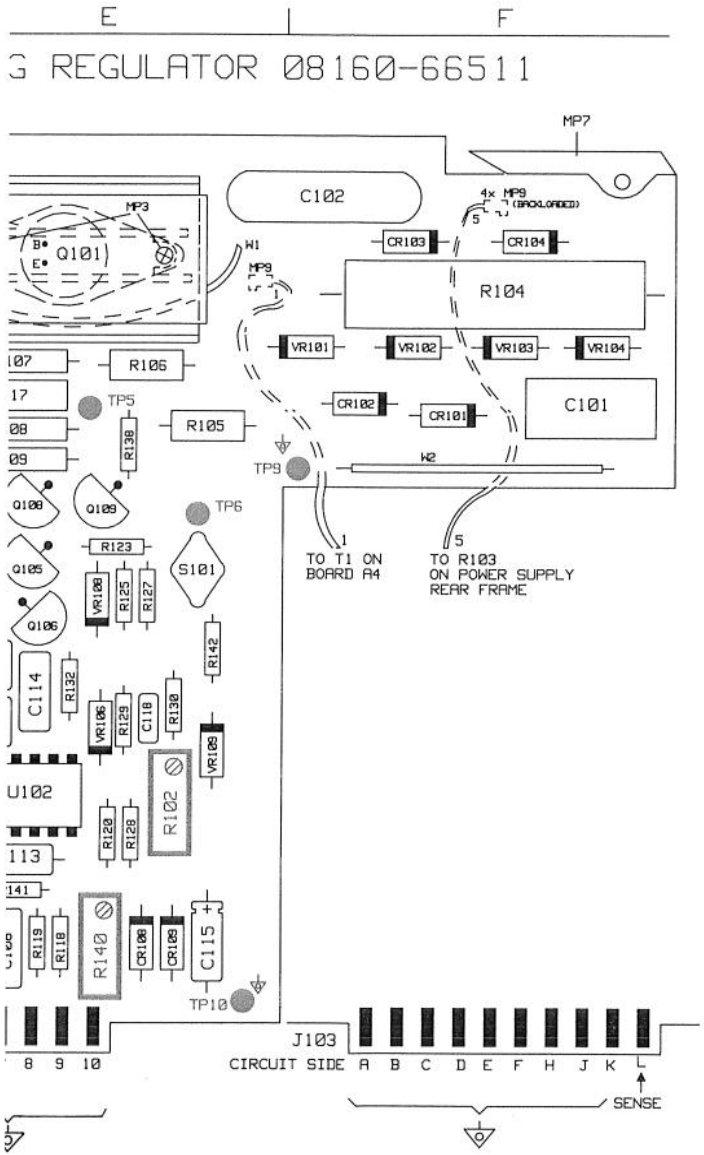
A10, Motherboard (Power Supply)
A11, Switching Regulator
A12, Rectifier
A13, Filter

COMPONENT LAYOUT DIAGRAMS

SCHEMATIC DIAGRAMS

FIGURES


A12 BD AY RECTIFIER 08160-66512
A11 BD AY SWITCHING REGULATOR
J102
INPUT
J101
OUTPUT
COMPONENT SIDE
CIRCUIT SIDE
J103
COMPONENT SIDE
N.C.
+40V +35V
TO R137 ON POWER SUPPLY REAR FRAME
CASE IS COLECTOR
MP5 SAFETY SHIELD
T101

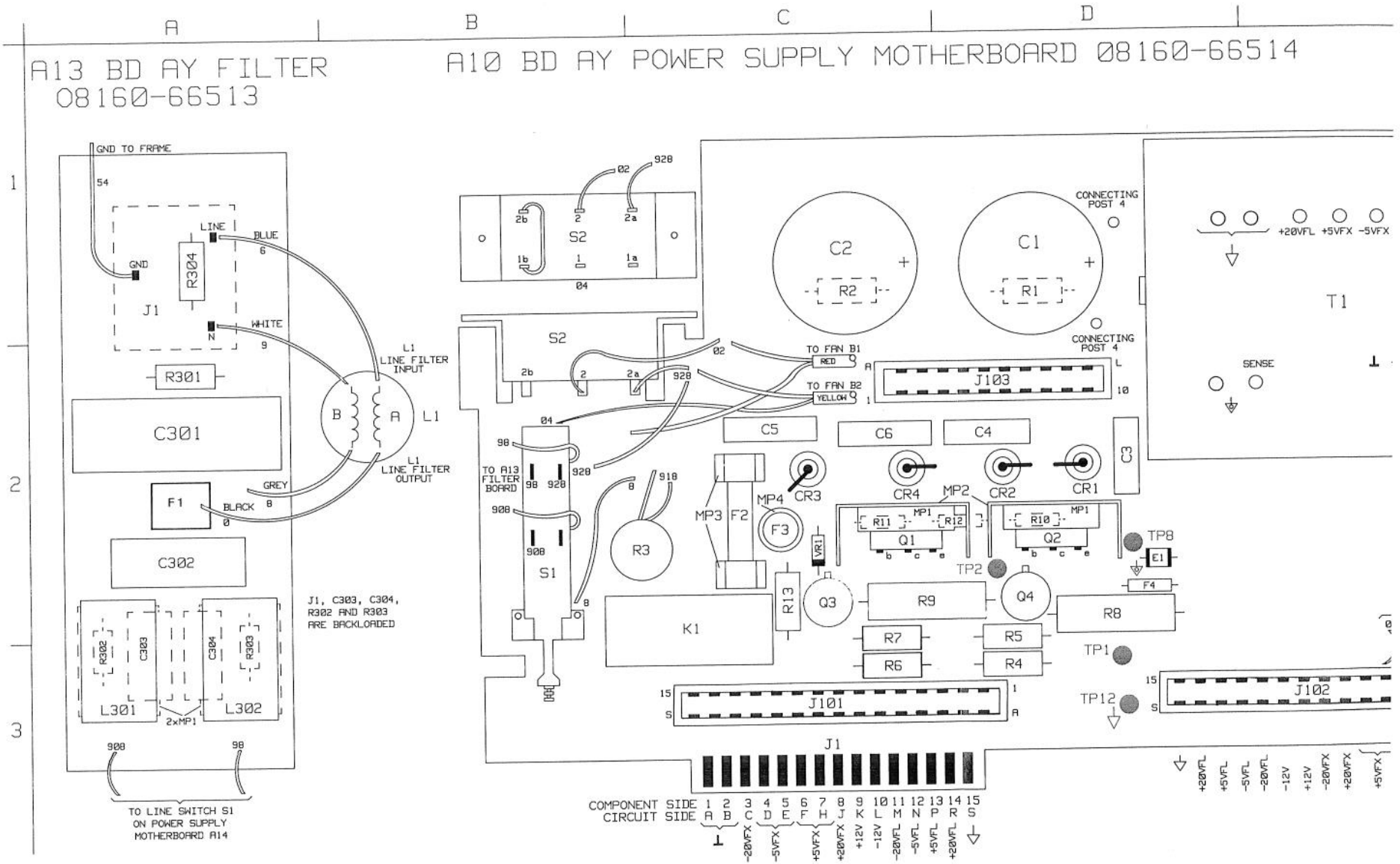


A12

REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
C201	B2	L210	C1
C202	B2	L211	C1
C203	B2	L212	C1
C204	B2	MP1	A1
C205	B2	MP2	B1/2
C206	B2	MP3	A1
C207	B1	MP4	C1
C208	B1	R201	C2
C209	B2	R202	C2
C210	B2	R203	C2
C211	B1	R204	C2
C212	B1	R205	C2
C213	B1	R206	C2
C214	B1	R207	C2
C215	B1	R208	C2
C216	B1	R209	C1
C217	B1	R210	C1
C218	B1	R211	B2
C219	C2	R212	A2
C220	C2	R213	B2
C221	C2	R214	A2
C222	C2	R215	B1
C223	C2	R216	A2
C224	C2	R217	A2
C225	C2	R218	A2
C226	C2		
C227	C1		
C228	C1		
C229	C2		
C230	B2		
C231	A2		
C232	B2		
C233	A2		
C234	B1		
C235	A2		
C236	A2		
C237	A2		
CR201	A2		
CR202	A2		
CR203	A2		
CR204	A2		
CR205	B1		
CR206	A1		
CR207	A2		
CR208	A2		
CR209	A1		
CR210	A1		
F201	C2		
F202	C2		
L201	B2		
L202	B2		
L203	B2		
L204	C2		
L205	C1		
L206	A1		
L207	A2		
L208	A2		
L209	C1		

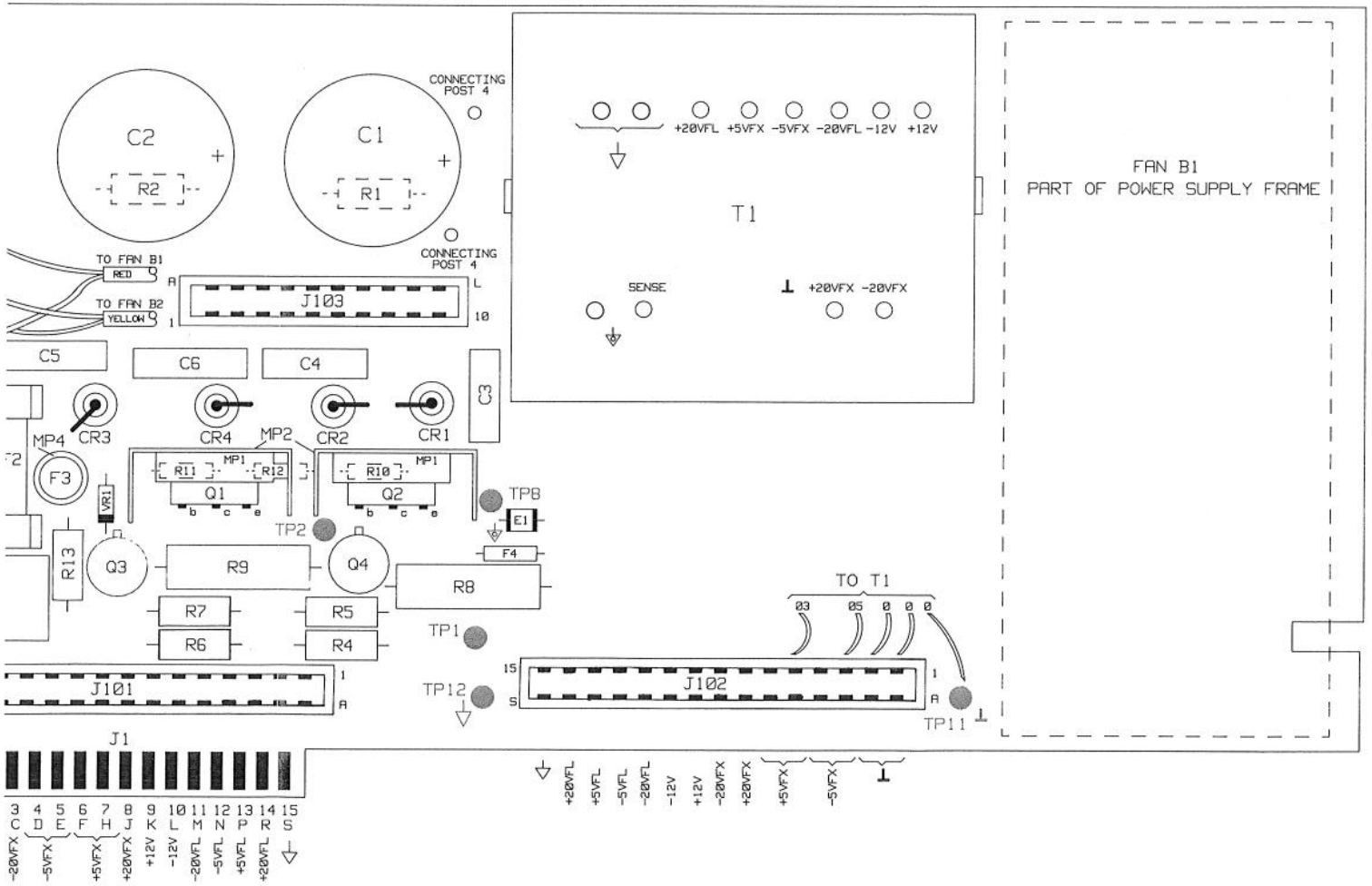
A11

REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
C101	F1	R110	D2
C102	F1	R111	D2
C103	D2	R112	D2
C104	D2	R113	D3
C105	D2	R114	D2
C106	D2/3	R115	D2
C107	D2/3	R116	D3
C108	E3	R117	D3
C109	E2	R118	E3
C110	E2	R119	E3
C111	D2	R120	E3
C112	E3	R121	E2
C113	E3	R122	E2
C114	E2	R123	E2
C115	E3	R124	E2
C116	D3	R125	E2
C117	E1	R126	E2
C118	E2	R127	E2
C119	E2	R128	E3
C120	D2	R129	E2
CR101	F2	R130	E2
CR102	F1	R131	E3
CR103	F1	R132	E2
CR104	F1	R133	E2
CR105	D3	R134	D2
CR106	E3	R135	D3
CR107	D3	R136	D3
CR108	E3	R138	E2
CR109	E3	R139	E2
		R140	E3
L101	D1	R141	E3
L102	D2	R142	E2
L103	D3	RT101	E3
MP1	E1	S101	E2
MP2	D1	T101	D2
MP3	E1	TP3	D3
MP4	E1	TP4	D2
MP5	D/E1	TP5	E2
MP6	D1	TP6	E2
MP7	D1	TP7	D2
MP9	F1	TP9	E2
Q101	D1	TP10	E3
Q102	E1	U101	D/E3
Q103	D2	U102	E3
Q104	D2	U103	D2
Q105	E2	VR101	F1
Q106	E2	VR102	F1
Q107	E2	VR103	F1
Q108	E2	VR104	F1
Q109	E2	VR105	D2
Q110	D2	VR106	E2
R101	D3	VR107	D3
R102	E3	VR108	E2
R104	F1	VR109	E2
R105	E2		
R106	E1		
R107	E1		
R108	E2		
R109	E2		


A13 BD AY FILTER
08160-66513
A10 BD AY POWER SUPPLY MOTHERBOARD 08160-66514
GND TO FRAME
54
LINE
BLUE
6
GND
R304
J1
WHITE
N
9
L1
LINE FILTER
INPUT
R301
C301
B
A
L1
L1
LINE FILTER
OUTPUT
GREY
F1
BLACK
8
C302
R302
C303
C304
R303
L301
L302
2xMP1
J1, C303, C304,
R302 AND R303
ARE BACKLOADED
908
98
TO LINE SWITCH S1
ON POWER SUPPLY
MOTHERBOARD A14
S2
02
928
2b
2
2a
1b
1
1a
04
TO A13
FILTER
BOARD
98
928
908
S1
8
918
R3
K1
C2
R2
C1
R1
CONNECTING
POST 4
TO FAN B1
RED
TO FAN B2
YELLOW
J103
10
C5
C6
C4
C3
CR4
CR2
CR1
MP4
CR3
MP3
F2
F3
MP2
MP1
R11
R12
R10
Q1
Q2
b
c
e
TP2
TP8
E1
F4
VR1
R13
Q3
R9
Q4
R8
R7
R5
R6
R4
TP1
TP12
J101
J102
15
S
1
A
T1
SENSE
+20VFL
+5VFX
-5VFX
J1
COMPONENT SIDE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
CIRCUIT SIDE A B C D E F H J K L M N P R S
-20VFX
-5VFX
+5VFX
+20VFX
+12V
-12V
-20VFL
-5VFL
+5VFL
+20VFL
+20VFL
+5VFL
-5VFL
-20VFL
-12V
+12V
-20VFX
+20VFX
+5VFX

C | D | E | F

SUPPLY MOTHERBOARD 08160-66514



A13

REF. DES.	GRID LOC.
C301	A2
C302	A2
C303	A2/3
C304	A2/3
L301	A3
L302	A3
R301	A2
R302	A3
R303	A3
R304	A1

A10

REF. DES.	GRID LOC.
C1	D1
C2	C1
C3	D2
C4	D2
C5	C2
C6	C2
CR1	D2
CR2	D2
CR3	C2
CR4	C2
E1	D2
F2	C2
F3	C2
F4	D2
J101	C3
J102	E3
J103	D2
K1	C2/3
MP1	C/D2
MP2	C/D2
MP3	C2
MP4	C2
Q1	C2
Q2	D2
Q3	C2
Q4	D2
R1	D1
R2	C1
R3	B/C2
R4	D3
R5	D3
R6	C3
R7	C3
R8	D2
R9	C2
R10	D2
R11	C2
R12	D2
R13	C2
S1	B2
S2	B1
T1	E1
TP1	D3
TP2	D2
TP8	D2
TP11	E3
TP12	D3
VR1	C2

INTRODUCTION

The primary circuits operate as a switched mode DC-DC converter of the flyback type, which pre-regulates all outgoing secondary DC voltages.

The rectified line voltage is switched to flyback transformer T101 via the switching transistors A11/Q101 and Q102.

Feedback voltage is then routed to the switching control circuit, A11/U102, which controls the operation of the switching transistors by varying the pulse width.

Secondary circuits are for half-wave rectification and filtering.

The Switched Supply consists of the following circuits:

1. Primary Circuits
   - A. A13-Filter Board, Line Input Filter
   - B. A10-Power Supply Motherboard
     - 1.) Voltage Selector
     - 2.) Current Limiter
     - 3.) Rectifier
     - 4.) Fans
     - 5.) Start Circuit
   - C. A11-Switching Regulator
     - 1.) Feedback Rectifier
     - 2.) +12 V Supply
     - 3.) Switching Control and Alarm
     - 4.) Drive Current
     - 5.) Duty Cycle Correction
     - 6.) Driver Stage
     - 7.) Switching Circuit
2. Secondary Circuits
   - A. Rectifier
   - B. Charging Capacitor
   - C. LC Circuit (ripple)
   - D. Discharge Capacitor (bleeder resistor)

PRIMARY CIRCUITS

Line Input Filter (A13)

The line input filter consists of the following:

1. RFI Filter: C301, 2, 3, and 4, L1, L301, and L302
2. Resonance Damp: R302, R303, L301, and L302
3. Discharge Resistors: R301 and R304
4. Fuse F1: protects the instrument from overloads and short circuits.

Voltage Selector, Current Limiter, Rectifier, and Fans (A10)

Instrument operation is activated via the front panel line switch, S1.

The line voltage range is selected via the line voltage selector switch, S2.

In the 115 V position of S2, rectifier diodes CR1 and CR4 are connected to charging capacitors C1 and C2 to form a voltage doubler.

In the 230 V position of S2, rectifier diodes CR1-CR4 form a bridge.

The fans are in parallel in the 115 V mode and in series in the 230 V mode.

At power-on, the charging current of C1 and C2 is limited by R3 to protect S1, CR1, CR3, and CR4 from current spikes.

R3 is itself protected during power-on by F2 which is bypassed in normal operation by relay K1 which is activated by a feedback voltage from CR108 and C116.

The rectified line voltage across C1 and C2 is 200 V to 358 V. To prevent this rectified AC voltage from damaging the start supply during incorrect operation, for example, incorrect line voltage, overvoltage protector E1 ignites and short circuits the input circuit and blows fuse F1 or F2.

CAUTION

Power-on with the incorrect line voltage selected blows either F1 or F2. Only after unplugging the instrument from the power source and correctly selecting the line voltage are the fuses to be checked and replaced.

Start Circuit (A10)

The start circuit delivers power for the control circuits during the following three phases of supply operation:

1. Start phase
2. After an alarm and until the next soft start
   Soft start is defined in the Switching Control and Alarm Circuits section that follows.
3. After final alarm blocking and until supply power-off.

The cascaded Darlington emitter-followers deliver 35 V DC from VR1. When the supply reaches its normal operating state, the start circuit is decoupled from the circuit by the "or" action of CR106 and CR107 since the feedback voltage from CR108 and C116 is now more positive (approximately 40 V).

Fuse F3 protects the start circuit from overload conditions.

Feedback Rectifier (A11)

The sense winding on the flyback transformer senses the rectified line voltage and the load conditions. Thus, it provides two paths of feedback rectification:

1. In normal operation, CR108 and C116 produce the supply voltage for the drive stage, the 12V regulator IC U101 and relay K1 (This supply is selected, as opposed to the start supply, because of the "or" action of CR106 and CR107 which select the more positive voltage.

2. CR 109 and C115 generate the feedback sensing voltage which is then divided by R128 and R129 and R102 before conparison with the reference voltage of VR6. This comparison is accomplished via the switching control circuit U102 which then provides voltage regulation. Potentiometer R102 determines the feedback voltage level and all output voltages.

+12 Volt Supply (A11)

Zener diode VR107 reduces the voltage at U101/1 to the U101 operating range. U101 then stabilizes this voltage to supply +12 V to the switching control circuit U102, alarm circuits, and the duty cycle monostable circuit U103.

Switching Control and Alarm Circuits (A11)

Figure 1, page 3.2-16, is a block diagram of the switching control IC, A11/U102.

1. The Miller integrator generates a sawtooth waveform at pin 3 with a frequency determined by R119 and C108.

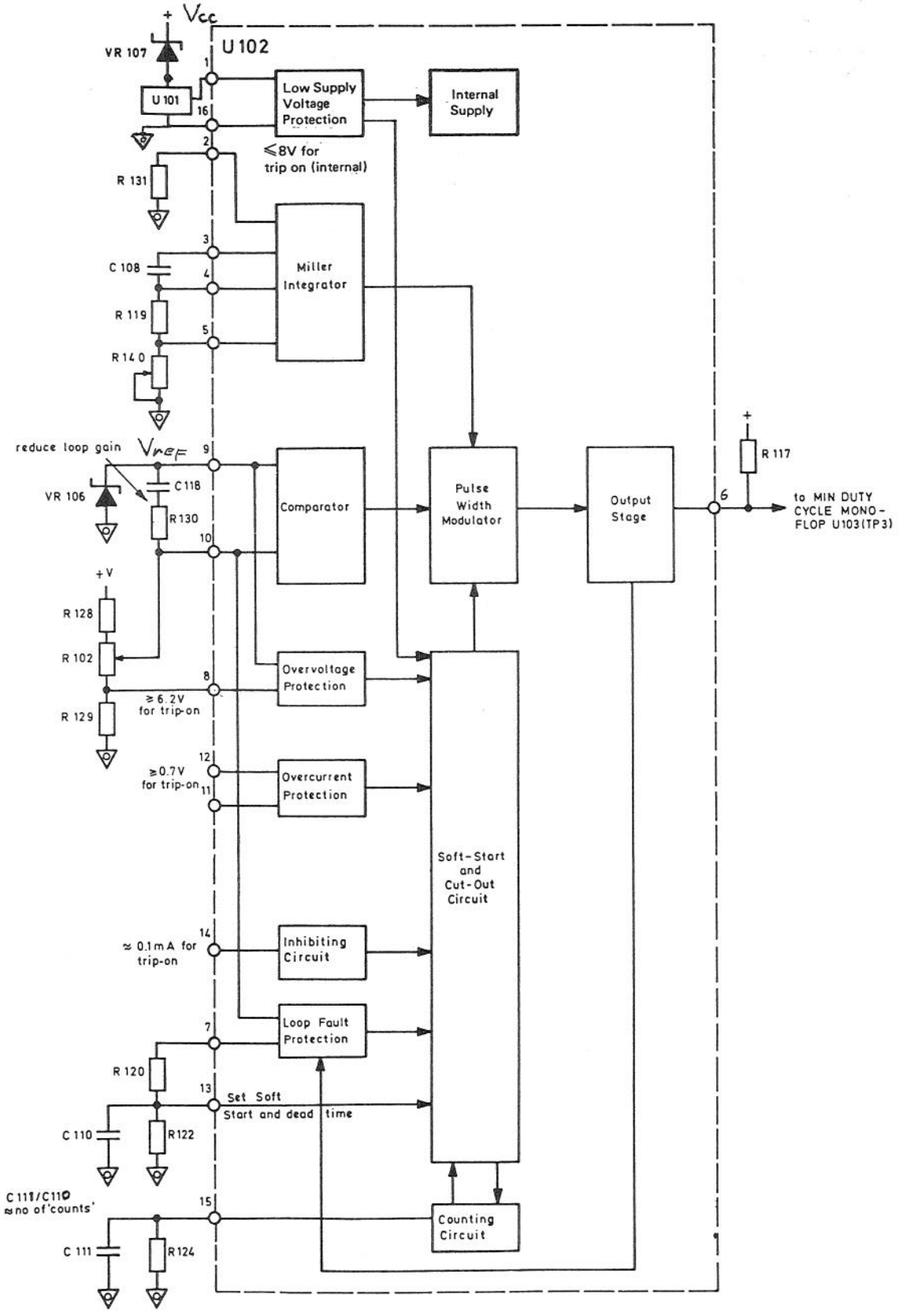
2. The comparator compares the feedback sensing voltage from divider R128, R129 and R102 with the reference voltage from VR106. R130, C118, C114 and the source resistance of the voltage divider serve to reduce the loop gain.

3. The pulse width modulator compares the sawtooth waveform with the comparator output signal to provide pulse width variation.

4. The soft-start and cutout circuit receives the alarm signals from the protection circuits (over-voltage and over-current, etc.) and subsequently controls the pulse width modulator to achieve soft-start (slowly increasing width) or cutout. R122 and C110 determine the dead time and soft-start time which occurs after supply start-on or after an alarm. During dead time, the operating cycle is held to zero and is then slowly increased during soft-start to achieve the required value for normal operation.

5. The number of alarms is limited by the voltage of C111 (TP7). In normal operation this voltage is approximately 1.6 V to 1.8 V. After each alarm, this voltage steps up by an amount determined by the ratio of C111/110. When the trip level, 5 V, is reached, a final step to 6.2 V occurs which blocks further operation. This state is called 'final alarm' and to remove this blocking action, the instrument must be switched off for 5 seconds to discharge C111.

FIGURE 1. SWITCHING CONTROL IC, A11/U102.



6. Over-current alarm occurs when a voltage of 0.65 V to 0.75 V exists between pins 11 an 12 of U102.

   Over-voltage alarm occurs when the voltage at pin 8 is => 6.2 V.

   Low supply voltage alarm occurs when the voltage at pin 1 is <= 8 V.

   Loop fault protection occurs when the feedback loop is open or short circuited. The duty cycle is then reduced to zero. After the dead time, the duty cycle rises to a value of duty cycle (open) which is determined by R120. It is held at this value until the loop is restored. Then it rises with a soft-start to the operating value. To prevent loop fault during start-on under heavy load, VR109 shifts the feedback voltage on pin 10 to 3.75 V.
7. The output stage consists of a common emitter stage with an open collector clamped to +12 V. R117 is a pull-up resistor.

Over Current Alarm Circuit (A11)

Current through the switching transistors Q101 and Q102 is sensed by R105 and R106. The differential stage Q108 and Q109 then compares this signal with the voltage determined by voltage divider R126 and R139. The over-current alarm is sensed by U102 pin 12 at Q108's collector.

Over Temperature Alarm Circuit (A11)

Thermal switch S101 closes when the air temperature reaches 71 degrees C. ± 2.5 degrees C. and starts an alarm on the overcurrent alarm line.

Over Voltage Alarm Circuit (A11)

The low end of the voltage adjust potentiometer R102 is connected to U102 pin 8 (over-voltage alarm). Thus, R102 must be set slightly above the low end to avoid false alarms occuring during normal operation.

Drive Current (A11)

To ensure an infinite final alarm blocking state without damage to the starting circuit which is supplying the required current in this state, it is necessary to reduce the load current drawn by the drive stage (Q101, Q102 = off and Q103 = on).

The differential stage Q105 and Q106 senses the alarm counting voltage an TP7 (C111, U102 pin 15) and compares it with the reference voltage from VR106 and U102 pin 9.

In normal operation, Darlington transistor Q105 and Q107 and Q110 conduct providing the normal drive current and bypassing R135. If a final alarm occurs, the voltage at TP7 becomes equal to that of VR106 and Q105, Q107, and Q110 are turned off. R135 then reduces the steady state drive current and VR 108 enables oscillation free clipping.

Duty Cycle Correction (A11)

U102 delivers a duty cycle of 20-90%. However, the switching transistors require a duty cycle of 2-45%. Therefore, a correction must be made.

1. Minimum duty cycle. The switching signal from U102 pin 6 (TP3) is fed through the minimum duty cycle monostable vibrator formed by NOR gates U103 pins 1,2,3 and U103 pins 11,12,13. The unstable on-time is adjustable via R101. This time is then subtracted by NOR gate U103 pins 8,9,10 from the original switching signal (U102) to obtain a signal at U103 pin 10 with the required duty cycle.
2. Maximum duty cycle. The maximum duty cycle is limited by R118, R140, R141, RT101 and adjusted with R140.

Driver Stage

The signal at TP4 is inverted by Q104 to control the drive transistor Q103. A103 then switches the operating feedback voltage of approximately 40 V to the flyback drive transformer T101. The secondary winding of T101 is connected to the base network of switching transistors Q101 and Q102. With this inductive loading, Q103 is protected by C104, R110, and VR105. R134 limits the steady state drive current while C103 lowers the impedance to obtain the required current pulses.

The winding polarity of T101 is designed to give a positive base voltage at Q101 and Q102 with a rising voltage at the collector of Q103. The winding ratio at T101 is 10:1.

Switching Circuit

Transistors Q101 and Q102 are connected in parallel and switch the primary winding of main flyback transformer T101 to the rectified line voltage of C1 and C2.

During the transistor on-time, current rises linearly to 10 A. At this point the secondary rectifiers are reverse biased.

After Q103 is switched on, the secondary stray inductance of T101, L101, L102, and L103 provides a controlled slow decrease of the base current in Q101 and Q102 during storage time. This continues until a negative base current I(B) is achieved which is approximately -2I(B).

At the same time the intrinsic collector region is fully discharged to ensure that the transistor's breakdown voltage can be achieved and thus reduce the power losses. Only when fully discharged, can Q101 and Q102 be cutoff.

Because cutoff energy is supplied by the base inductances L(S) of T101, L101, L102, and L103, a high di(B)/dt down to zero volts generates a high negative voltage spike which is added to the voltage at C117 and the transformer T101 reverse bias voltage. This brings the Q101 and Q102 base-emitter junctions into reverse breakdown to provide the fastest possible cutoff time (<0.8us) and so minimize the switching losses.

With Q101 and Q102 cutoff, the T101 secondary windings become forward biased. Energy is then discharged from the transformer, beginning with a high current and decreasing to zero before the next primary switch-on occurs.

To stay within the safe operating region of Q101 and Q102, a collector protection network is required.

As the Q101 and Q102 collector current decreases, the voltage rise is slowed down by charging capacitor C102 via CR103 and CR104 . Power switching losses are thus held to a minimum. C102 then discharges through R104, and CR103 and CR104 become reverse biased until transistors Q101 and Q102 switch on again.

The maximum value of the voltage spike at the Q101 and Q102 collector is limited by the peak charging current of C101 via CR101 and CR102. This charging takes place only for the duration of the spike, and C101 is discharged during the remainder fo the switching period via R103.

VR101 and VR104 clamp the spike at 720 V.

WARNING

Voltages in the collector network of Q101 and Q102 can rise to 750 while the rectified line voltage can reach 360 V with low impedance. The entire primary circuit is on a floating rectified line ground.

Service only with an isolation transformer to avoid danger to life and equipment.

SECONDARY CIRCUITS

The secondary windings of transformer T1 contain the windings required for all secondary voltages.

1. A fixed voltage group referenced to ground
2. A floating voltage group referenced to a voltage shifted from ground.

All secondary voltage circuits are identical, they consist of:

1. A one way rectifier with RFI suppression
2. A charging capacitor
3. An LC circuit to reduce ripple
4. A discharge resistor (bleed resistor).

Due to the 25 k Hz switching frequency, fast recovery diodes are used to reduce losses.

For the high current required in the ± 5 V fixed (fx) supplies, power Shottky diodes are used to reduce losses.

Charging capacitors with low equivalent series resistance are used.

POWER SUPPLY MODULE REMOVAL

Procedure:

a, Switch the instrument off.

b. Disconnect the line power cord from the instrument.

c. Remove three feet: two from the end frame at the top cover and the foot near the line voltage selector. Carefully remove the top cover; avoid damaging the top cover's RFI shielding.

d. Remove the three screws securing the power supply module. They are marked by white circles and the ATTENTION message.

e. **WARNING-the power supply module may be hot.** Slide the module out of the chassis; avoid damaging the RFI shielding, the fan cord and A11/J1.

TROUBLESHOOTING

The power supply contains two parts.

1. Switched supply-troubleshooting information is contained in this service block.
2. Power supply regulator(see Service Block 3).

Supply Voltages

The unregulated voltages can be measured on assembly A10. See Adjustment Procedure 1, Part 4 for instructions. Perform the procedure without making the adjustments.

The regulated voltages can be measured on the main motherboard. See Adjustment Procedure 2.

WARNING

Troubleshooting and adjustments within the switched supply must only be performed with a variable AC supply and an isolation transformer to provide galvanic seperation from the power source.

Voltages can be dangerous to life.
Work with extreme care in this area.

Switched Supply

The switched supply consists of 3 parts.

1. Power input, filter board A13 and power supply motherboard A10
2. Switching regulator, A11
3. Rectifier board, A12

± 5 V (fx) Fuses

If only the ± 5 V (fx) supplies are incorrect, check fuses A12/F201 and A12/F202.

Assembly A10 Troubleshooting

The following procedure is provided for troubleshooting the A10 assembly.

1. Switch the line power off.
2. Remove the power supply module from the instrument.
3. Remove boards A11 and A12 from the power supply.
4. Reconnect the line power cord.
5. Switch the instrument on.
6. Use a DVM with floating inputs and make the following measurements.

    a. Power Input Test:
    Measure between TP 8 (floating ground) and TP 1.

    The voltage range is 245V to 335 V depending on the line voltage.

    If out of range, check fuse F3, rectifier, and spark-gap.

    b. Start Voltage Test:
    Measure between TP 8 (floating ground) and TP 2.

    The voltage range is 35.5 V to 36.8 V depending on the line voltage.

    If out of range, check fuse F3 and Q1-Q4.

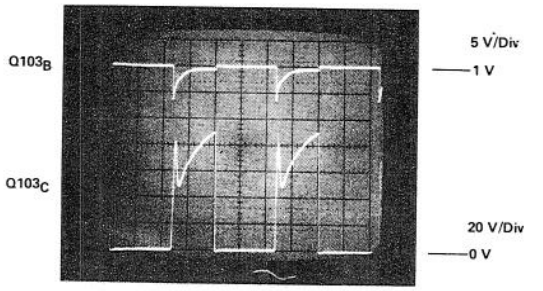
    NOTE: The test point locations are shown on the component layout diagram.

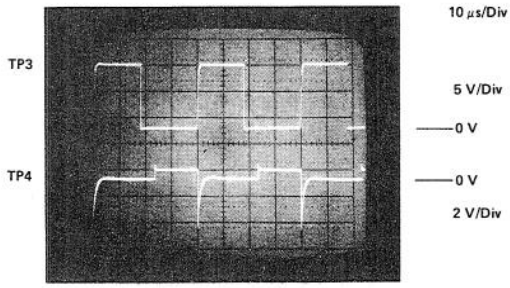
Assembly A11 Troubleshooting

The following procedure is provided for troubleshooting the A11 assembly.

1. Switch the line power off.
2. Remove the power supply module from the instrument.
3. Remove A11 from the power supply module.
   a. Disconnect wires 1 and 5.
   b. Leave wires 3 and 8 connected to the chassis mounted A11/R137.
   c. Connect the DC power supply
      1.) Negative pole (-) to A11/TP 10
      2.) Positive Pole (+) to the anode (+) of A11/CR108.
4. Set the DC power supply to 40 V.
5. Use a realtime scope and a 10:1 probe and measure the signals in Figures 2 and 3.

FIGURES 2A and 2B. STEP 5 SIGNALS.





6. Use a DVM with floating inputs and make the following measurements:

   a. Voltage Alarm-Normal State:
      Measure between TP 7 and TP 10.
      The voltage range is +1.6 V to +1.8 V.

   b. Under-voltage Alarm:
      Reduce the power supply voltage to 27 V - 30 V.
      Measure between TP 7 and TP 10.
      The voltage at TP 7 is +6.2 v (Alarm Value).

   c. Reset to Normal-Alarm State:
      Set the power supply voltage to 40 V.
      Turn the power supply off and then on again.
      The voltage measured between TP 7 and TP 10 is 1.6 to 1.8 V.

   NOTE: The test point locations are shown on the component layout diagram.

   d. Over-voltage Alarm:
      Set the power supply voltage to 45 V - 50 V.
      Measure the voltage between TP 7 and TP 10.
      The voltage at TP 7 is +6.2 V (Alarm Value).

   e. Repeat Step C (Reset to the normal state).

   f. Connect a second power supply as follows:
      1.) Negative pole (-) to TP 10
      2.) Positive pole (+) to TP 6

   g. Over-current Alarm:
      Set the second power supply to 0.5 V and slowly increase the voltage until the voltage at TP 7 is 6.2 V (Alarm Value).

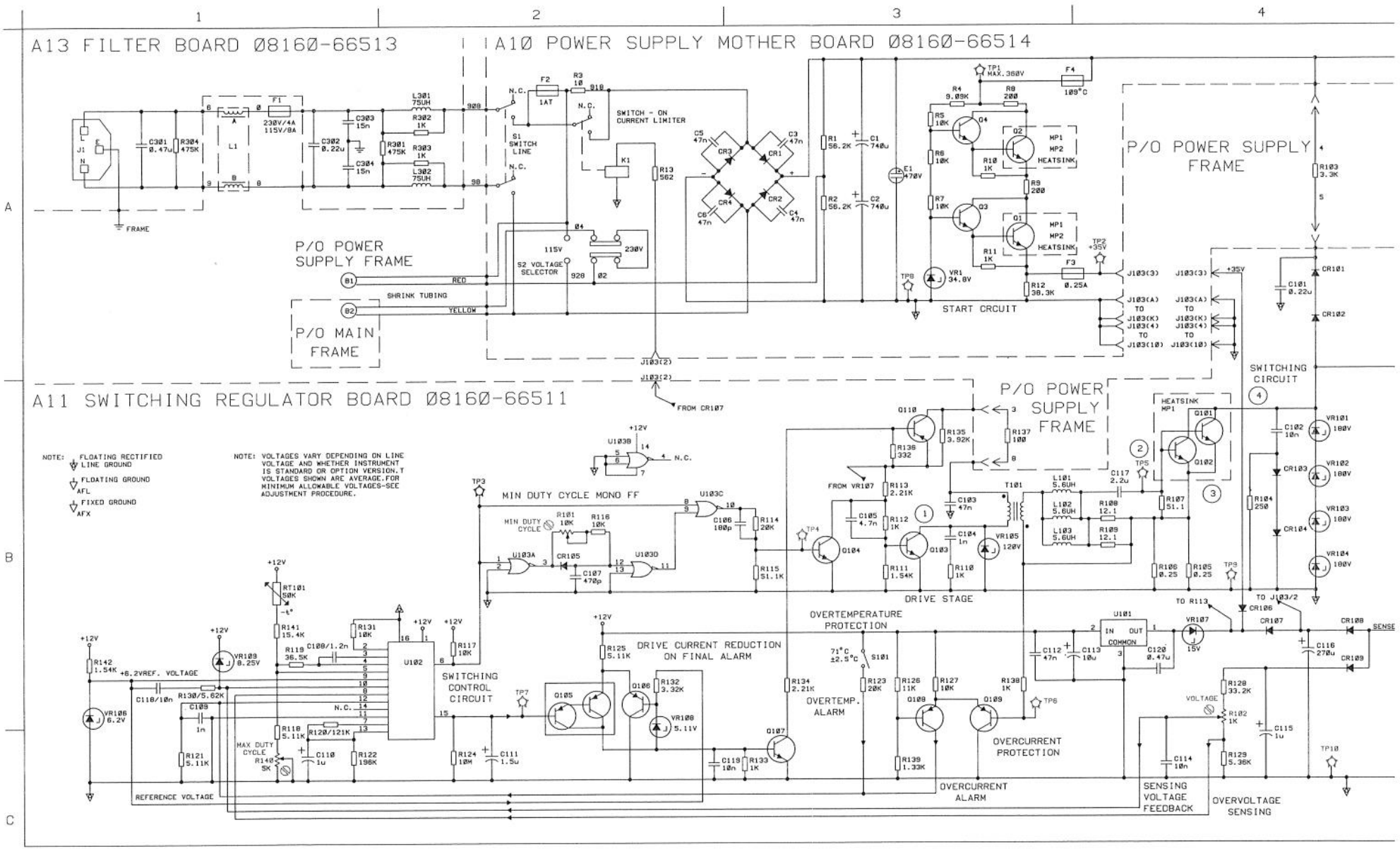
   h. Remove the second power supply.

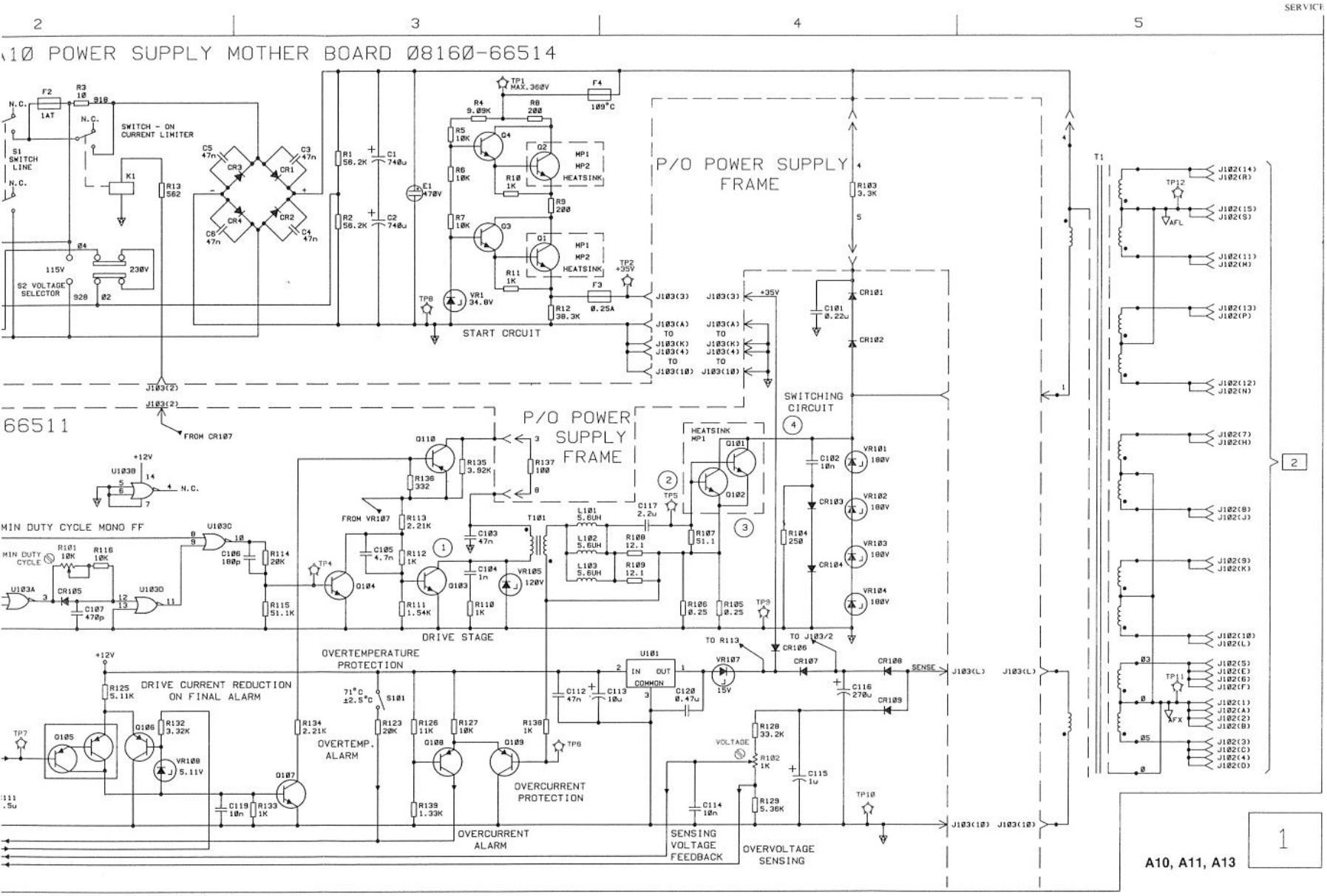
   i. Repeat Step C (Reset to the Normal State).

   j. Over-temperature Alarm:
      Heat the housing of S101 to 75-120 degrees C.
      The voltage at TP 7 is 6.2 V (Alarm Value).

      When the housing temperature returns to normal, repeat Step C (Reset to the normal state).

   NOTE: The voltage across A11/R137 is less than 0.2 V in the normal state. In any alarm state, it will increase to the supply voltage minus 2 V.


A13 FILTER BOARD Ø8160-66513
A1Ø POWER SUPPLY MOTHER BOARD Ø8160-66514
A11 SWITCHING REGULATOR BOARD Ø8160-66511
P/O POWER SUPPLY FRAME
P/O MAIN FRAME
SHRINK TUBING
RED
YELLOW
S1 SWITCH LINE
S2 VOLTAGE SELECTOR
SWITCH - ON CURRENT LIMITER
START CRCUIT
HEATSINK
SWITCHING CIRCUIT
NOTE: FLOATING RECTIFIED LINE GROUND
FLOATING GROUND AFL
FIXED GROUND AFX
NOTE: VOLTAGES VARY DEPENDING ON LINE VOLTAGE AND WHETHER INSTRUMENT IS STANDARD OR OPTION VERSION.T VOLTAGES SHOWN ARE AVERAGE.FOR MINIMUM ALLOWABLE VOLTAGES-SEE ADJUSTMENT PROCEDURE.
MIN DUTY CYCLE MONO FF
SWITCHING CONTROL CIRCUIT
DRIVE STAGE
OVERTEMPERATURE PROTECTION
DRIVE CURRENT REDUCTION ON FINAL ALARM
OVERTEMP. ALARM
OVERCURRENT PROTECTION
OVERCURRENT ALARM
SENSING VOLTAGE FEEDBACK
OVERVOLTAGE SENSING
REFERENCE VOLTAGE
FROM CR107
TO J103/2
TO R113
SENSE


2
3
4
5
A10 POWER SUPPLY MOTHER BOARD Ø8160-66514
P/O POWER SUPPLY FRAME
SWITCH - ON CURRENT LIMITER
START CRCUIT
SWITCHING CIRCUIT
P/O POWER SUPPLY FRAME
66511
FROM CR107
MIN DUTY CYCLE MONO FF
DRIVE STAGE
OVERTEMPERATURE PROTECTION
DRIVE CURRENT REDUCTION ON FINAL ALARM
OVERTEMP. ALARM
OVERCURRENT PROTECTION
OVERCURRENT ALARM
SENSING VOLTAGE FEEDBACK
OVERVOLTAGE SENSING
TO R113
TO J103/2
SENSE
HEATSINK MP1
HEATSINK MP2
A10, A11, A13
1
2

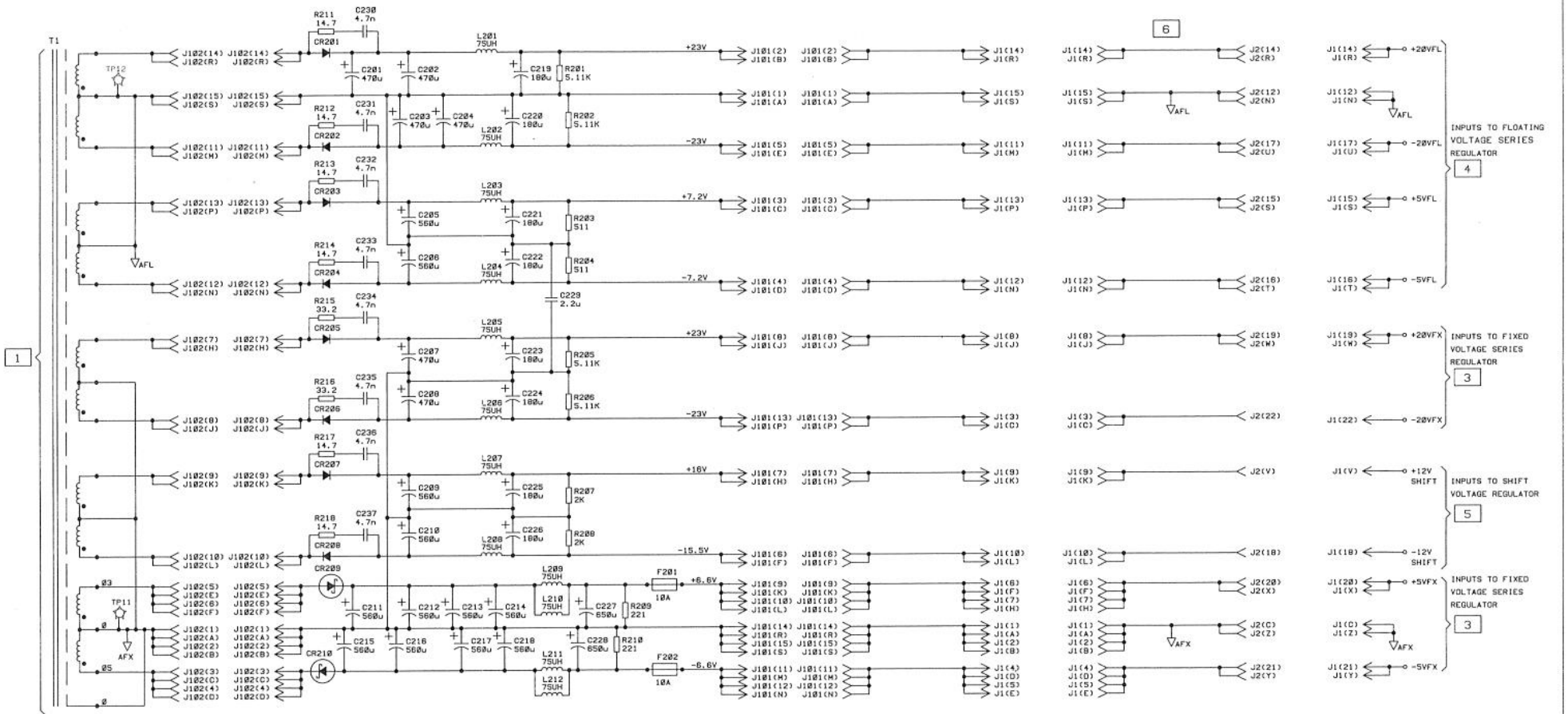
P/O A1Ø POWER SUPPLY MOTHER BD Ø8160-66514

A12 RECTIFIER BOARD Ø8160-66512

P/O A1Ø POWER SUPPLY MOTHER BD Ø8160-66514

P/O A1 MOTHER BD Ø8160-665Ø1

P/O A18 REGULATOR BD Ø8160-66518



NOTE: FLOATING GROUND
AFL
AFX

NOTE: VOLTAGES VARY DEPENDING ON LINE VOLTAGE AND WHETHER INSTRUMENT IS STANDARD OR OPTION VERSION. T VOLTAGES SHOWN ARE AVERAGE. FOR MINIMUM ALLOWABLE VOLTAGES-SEE ADJUSTMENT PROCEDURE.

A12

2

SB 3 SERIES VOLTAGE REGULATORS

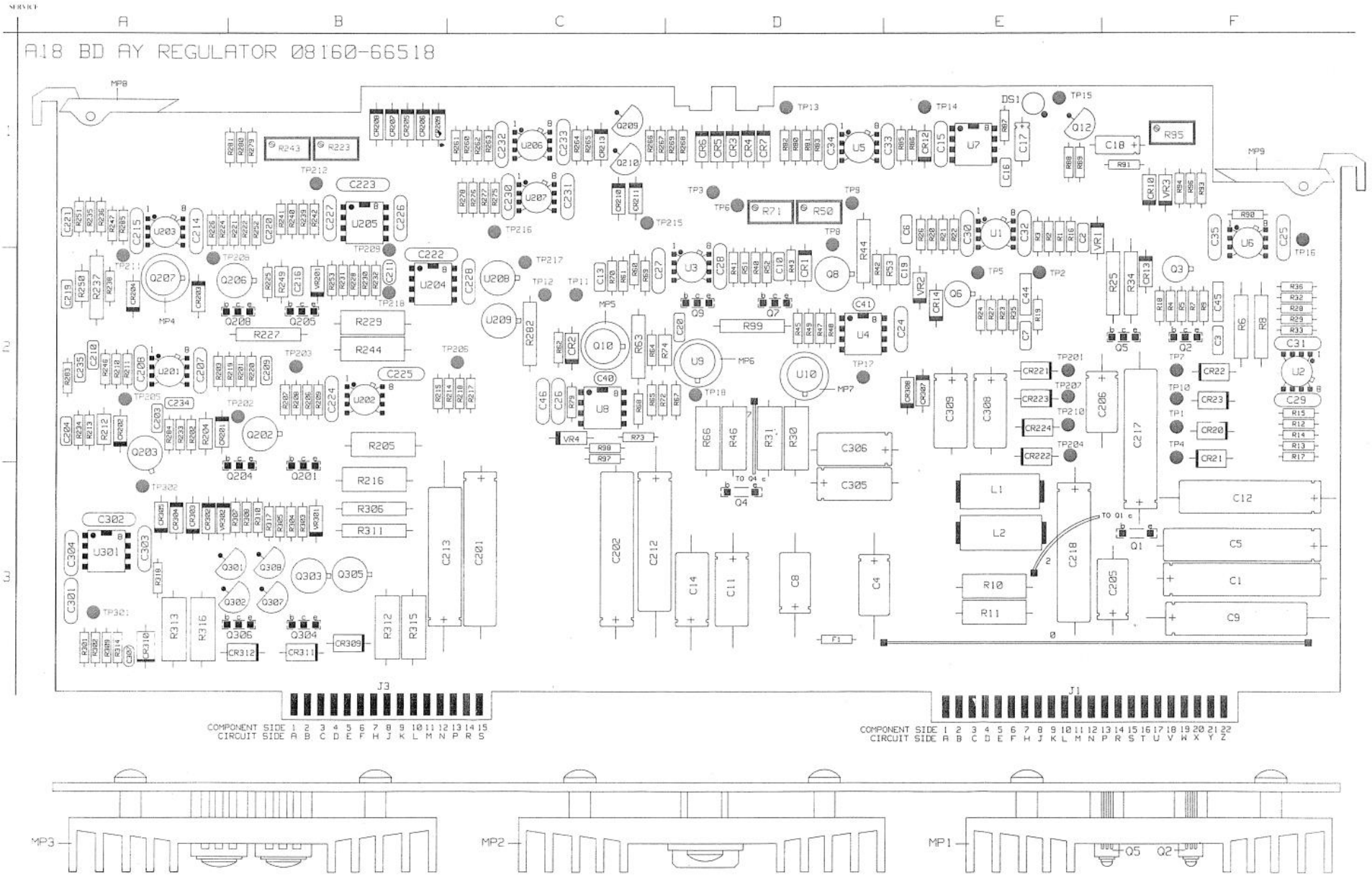
CONTENTS

ASSEMBLIES

COMPONENT LAYOUT DIAGRAM

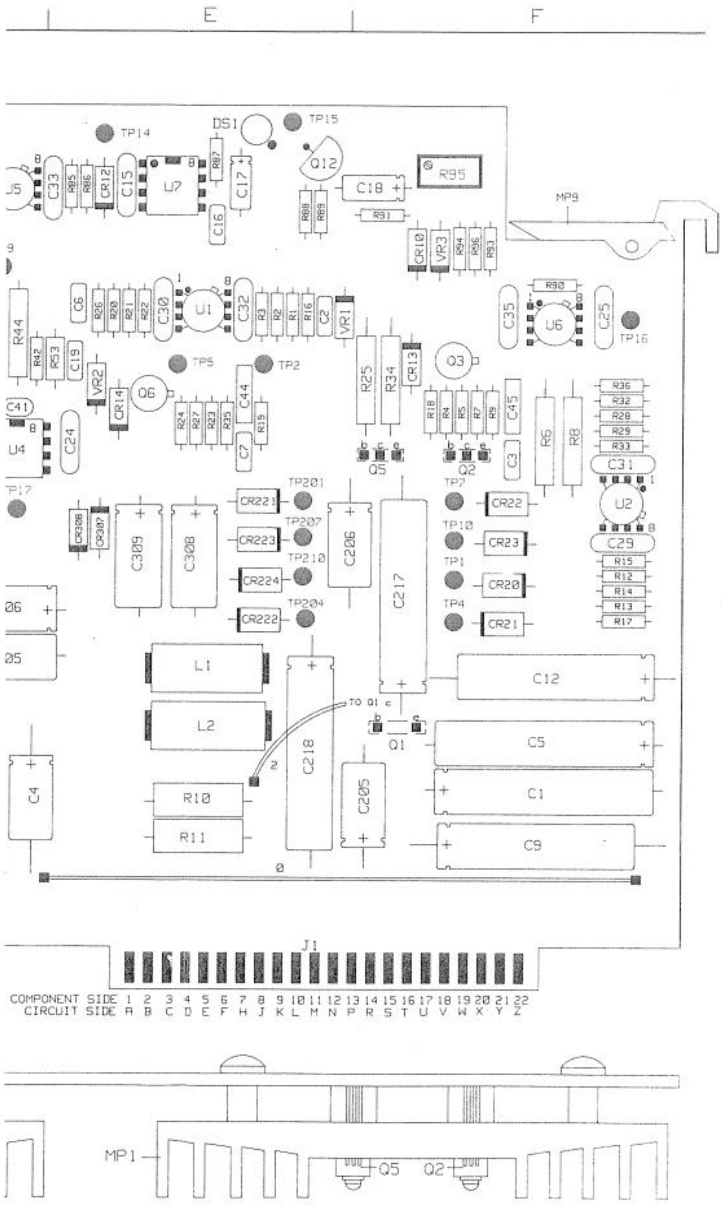
SCHEMATIC DIAGRAMS

FIGURE



REF DES

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C40 C41 C44 C45 C46 C201 C202 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 C216 C217 C218 C219 C220 C221 C222 C223 C224 C225 C226 C227 C228 C230 C231 C232 C233 C234 C235 C301 C302 C303 C304 C305 C306 C307 C308 C309 C310



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C1	F3	C218	E3	CR223	E2	Q306	B3	R61	C2	R223	B1	R306	B3	U6	F2
C2	E3	C219	A2	CR224	E2	Q307	B3	R62	C2	R224	A1	R307	B3	U7	E1
C3	F2	C220	B1	CR302	A3	Q308	B3	R63	C2	R225	B1	R308	B3	U8	C2
C4	D3	C221	A1	CR303	A3			R64	C2	R226	A1	R309	A3	U9	D2
C5	F3	C222	B2	CR304	A3	R1	E2	R65	C2	R227	B1	R310	B3	U10	D2
						R2	E2								
C6	E1	C223	B1	CR305	A3	R3	E2	R66	D2	R228	B2	R311	B3	U201	A2
C7	E2	C224	B2	CR307	E2	R4	F2	R67	D2	R229	B2	R312	B3	U202	B2
C8	D3	C225	B2	CR308	E2	R5	F2	R68	C2	R230	B2	R313	A3	U203	A1
C9	F3	C226	B1	CR309	B3			R69	C2	R231	B2	R314	A3	U204	B2
C10	D2	C227	B1	CR310	A3	R6	F2	R70	C2	R232	B2	R315	B3	U205	B1
				CR311	B3	R7	F2								
C11	D3	C228	C2	CR312	B3	R8	F2	R71	D1	R233	A2	R316	A3	U206	C1
C12	F3	C230	C1			R9	F2	R72	C2	R234	A2	R317	B3	U207	C1
C13	C2	C231	C1	DS1	E1	R10	E3	R73	C2	R235	A1	R318	A3	U208	C2
C14	D3	C232	C1					R74	C2	R236	A1			U209	C2
C15	E1	C233	C1	F1	D1	R11	E3	R79	C2	R237	A2	TP1	F2	U301	A3
						R12	F2					TP2	E2		
C16	E1	C234	A2	J2	F1	R13	F2	R80	D1	R238	A1	TP3	D1	VR1	E2
C17	E1	C235	A2			R14	F2	R81	D1	R239*	B1	TP4	F2	VR2	E2
C18	E1	C301	A3	L1	E3	R15	F2	R82	D1	R240	B1	TP5	E2	VR3	F1
C19	E2	C302	A3	L2	E3			R83	D1	R241	B1			VR4	C2
C20	D2	C303	A3			R16	E2	R85	E1	R242	B1	TP6	D1	VR201	B2
				MP1	E/F3	R17	F2					TP7	F2		
C24	E2	C304	A3	MP2	C/D3	R18	F2	R86	E1	R243	B1	TP8	D2	VR301	B3
C25	F2	C305	D3	MP3	A/B3	R19	E2	R87	E1	R244	B2	TP9	D1	VR302	A3
C26	C2	C306	D3	MP4	A2	R20	E2	R88	E1	R246	A2	TP10	F2		
C27	C2	C307	A3	MP5	C2			R89	E1	R247	A1				
C28	D2	C308	E2			R21	E2	R90	F2	R249	B2	TP11	C2		
		C309	E2	MP6	D2	R22	E2					TP12	C2		
C29	F2			MP7	D2	R23	E2	R91	F1	R250	A2	TP13	D1		
C30	E2	CR1	D2	MP8	A1	R24	E2	R93	F1	R251	A1	TP14	E1		
C31	F2	CR2	C2	MP9	A1	R25	F2	R94	F1	R252	B1	TP15	F1		
C32	E2	CR3	D1					R95	F1	R253	B2				
C33	E1	CR4	D1	Q1	F3	R26	E2	R96	F1	R260	C1	TP16	F1		
		CR5	D1	Q2	F2	R27	E2					TP17	D2		
C34	D1			Q3	F2	R28	F2	R97	C3	R261	C1	TP18	D2		
C35	F2	CR6	D1	Q4	D3	R29	F2	R98	C3	R262	C1	TP201	E2		
C40	C2	CR7	D1	Q5	F2	R30	D2	R99	D2	R263	C1	TP202	B2		
C41	D2	CR10	F1					R201	B2	R264	C1				
C44	E2	CR12	E1	Q6	E2	R31	D2	R202	A2	R265	C1	TP203	B2		
		CR13	F2	Q7	D2	R32	F2					TP204	E2		
C45	F2			Q8	D2	R33	F2	R203	A2	R266	C1	TP205	A2		
C46	C2	CR14	E2	Q9	D2	R34	F2	R204	A2	R267	C1	TP206	C2		
C201	C3	CR20	F2	Q10	C2	R35	E2	R205	B2	R268	D1	TP207	E2		
C202	C3	CR21	F3					R206	B2	R269	D1				
C203	A2	CR22	F2	Q12	E1	R36	F2	R207	B2	R275	C1	TP208	A2		
		CR23	F2	Q201	B2	R40	D2					TP209	B2		
C204	A2			Q202	B2	R41	D2	R208	B2	R276	C1	TP210	E2		
C205	F3	CR201	A2	Q203	A2	R42	D2	R209	B2	R277	C1	TP211	A2		
C206	F2	CR202	A2	Q204	B2	R43	D2	R210	A2	R278	C1	TP212	B1		
C207	A2	CR203	A2					R211	A2	R279	B1				
C208	A2	CR204	A2	Q205	B2	R44	D2	R212	A2	R280	B1	TP215	C1		
		CR205	B1	Q206	B2	R45	D2					TP216	C1		
C208	A2			Q207	A2	R46	D2	R213	A2	R281	B1	TP217	C2		
C209	B2	CR206	B1	Q208	B2	R47	D2	R214	C2	R282	C2	TP218	B2		
C210	A2	CR207	B1	Q209	C1	R48	D2	R215	B2	R283	A2	TP301	A3		
C211*	B2	CR208	B1					R216	B3	R284	A2	TP302	A3		
C212	C3	CR209	B1	Q210	C1	R49	D2	R217	C2	R285	A1				
		CR210	C1	Q301	B3	R50	D1								
C213	B3			Q302	B3	R59	D3	R218	C2	R301	A3	U1	E2		
C214	A1	CR211	C1	Q303	B3	R51	D2	R219	B2	R302	A3	U2	F2		
C215	A1	CR213	C1	Q304	B3	R52	D2	R220	B2	R303	B3	U3	D2		
C216	B2	CR221	E2	Q305	B3	R53	E2	R221	B1	R304	B3	U4	D2		
C217	F2/3	CR222	E2			R60	C2	R222	B1	R305	B3	U5	D1		

INTRODUCTION

The regulator assembly, A18, consists of three sections.

1. Fixed Voltage Supply
2. Floating Voltage Supply
3. Shift Voltage (described in Service Block 12.

FIXED VOLTAGE SUPPLY

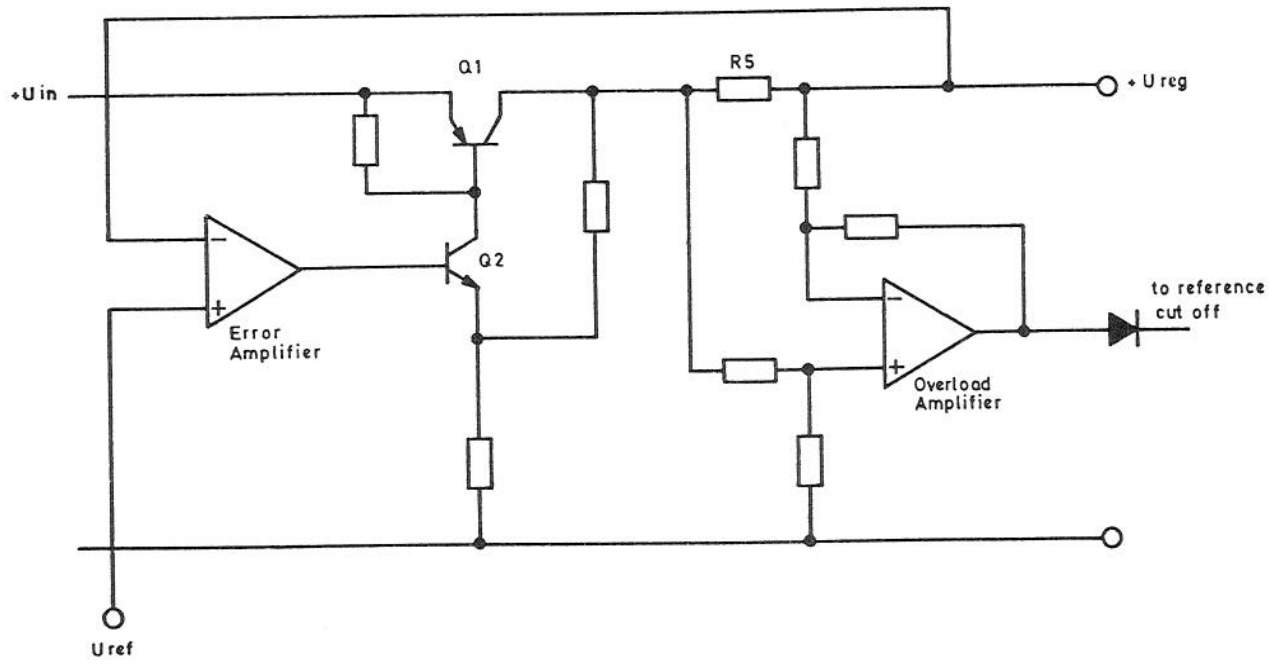
This section provides four voltages referenced to ground.

The regulators are based on the same principle which is shown in the following figure.

The error amplifier compares Vreg with Vref and drives the regulator transistor Q1 to zero difference.

Excessive output current is then detected by R5 and the overload amplifier. The output of the overload amplifier goes high if an overload occurs.

FIGURE 1. FIXED VOLTAGE SUPPLY



Reference Voltage Circuit

The reference voltage for the +5 V fixed supply is derived from the temperature compensating diode A18/VR3.

The Zener voltage is divided by A18/R94, R95, and R96 to +5 V and then converted via A18/U6 to a low impedance.

To obtain good tracking, the +5 V fixed regulator output is used as a reference input for the -5 V fixed supply.

The -5 V fixed regulator output is then used as a reference input for the ± 20 V fixed supplies.

Reference Shut-down Circuit

An overload signal from an overload amplifier cuts off diode A18/CR7 and the inverting input of U5 goes high. The output of U5 goes low and triggers the timer.

The timer then drives Q12 which shorts the reference voltage causing all regulated voltages to go down.

The shutdown state is indicated by an LED, DS1, on the regulator board.

After a run-down time determined by the time constant of A18/R87 and A18/C17, the timer output goes low and cuts off Q12.

If the overload condition persists, the shutdown sequence is repeated.

FLOATING VOLTAGE SUPPLY

The floating voltage circuits are based on the same principle as the fixed voltage circuits except they are referenced to floating ground.

SHIFT VOLTAGE

See Service Block 12.

TROUBLESHOOTING

Two basic faults can appear in the fixed or floating voltage supplies.

1. No voltage or over voltage caused by a faulty regulator circuit.
2. Excessive current caused by a failure on another board.

Alarm LED Status

If the LED is flashing, all voltages will be down. This state is caused by a supply overvoltage or excessive current. Off is the normal condition.

Reference Shut-down Circuit Disabling

Transistor A18/Q12 is removed from its socket which opens the reference shutdown circuit and prevents the shorting of the reference voltage.

Isolate the output of the bad supply to prevent additional circuit damage.

PROCEDURE:

1. Connect the instrument to a variable AC power supply isolated from the line power by an isolation transformer.

2. Turn on the power supply to the selected line voltage. If excessive current flows, switch the instrument off, and troubleshoot the power supply module.

3. If the Alarm LED is not flashing, measure the voltages to find the fault.

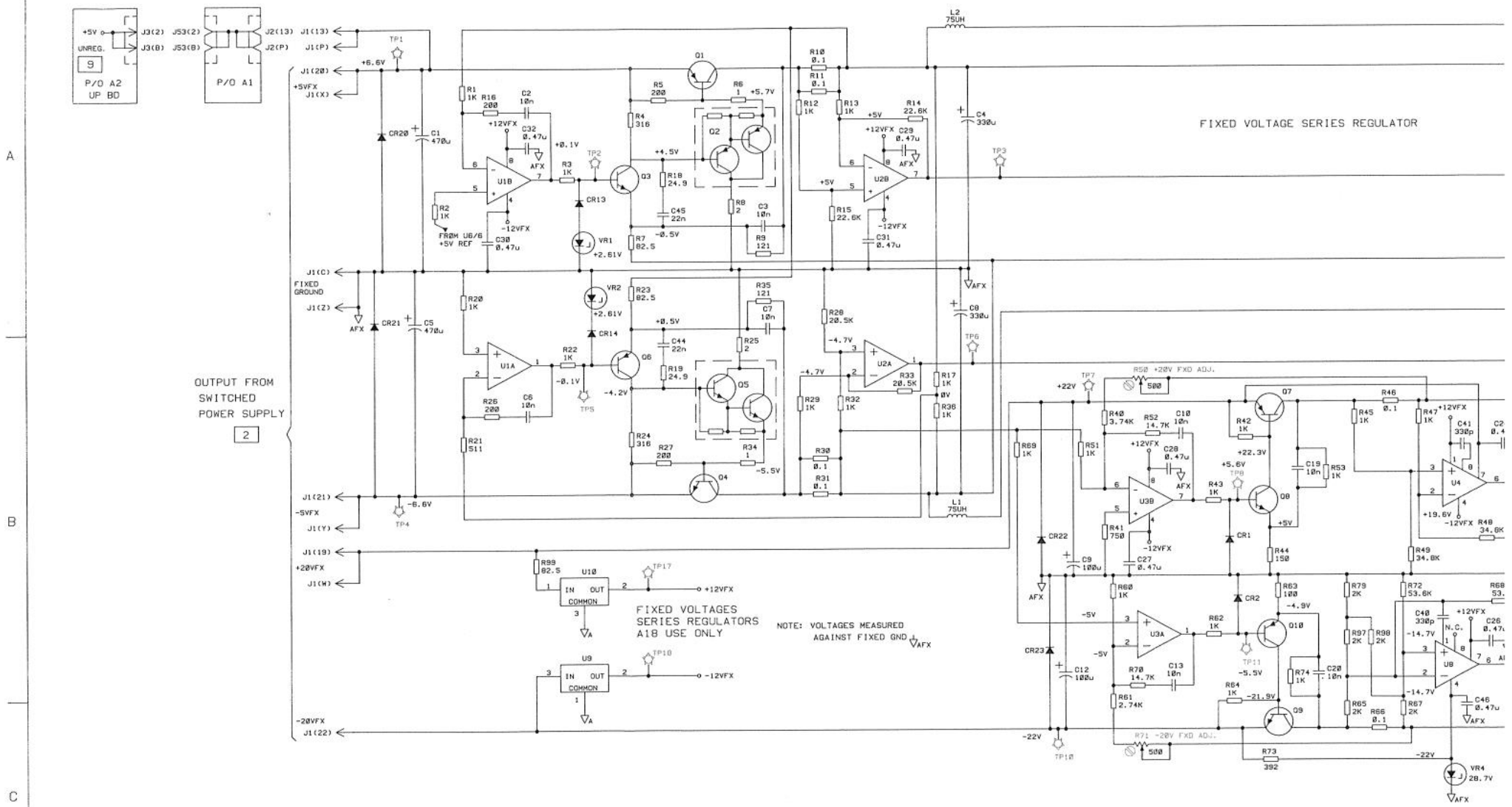
4. If the Alarm LED is flashing, check for an over-voltage condition. Troubleshoot the related ciruit if an over-voltage is found.

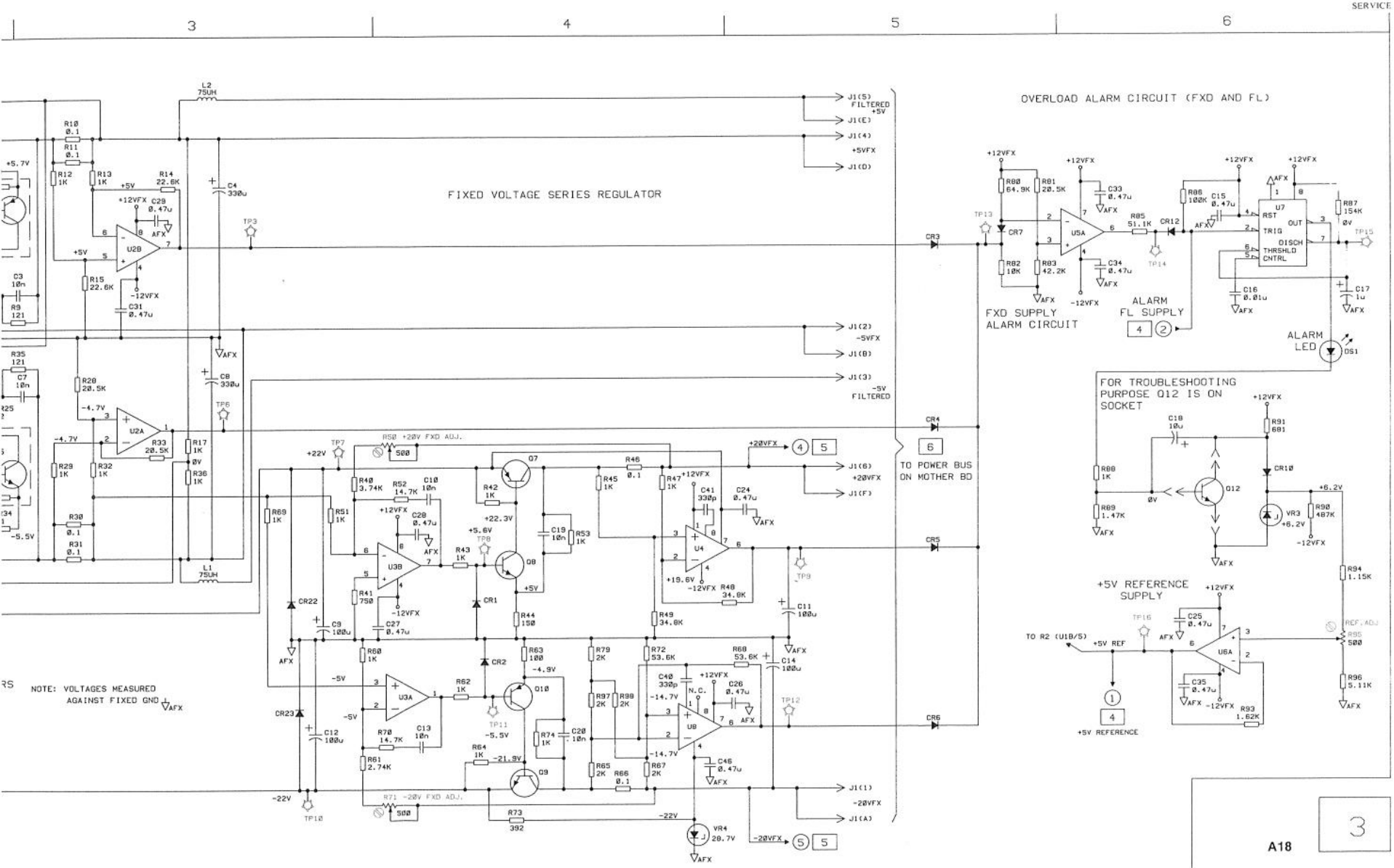
5. If an overvoltage condition is not found, measure TP 13 and TP 215 to determine whether a fixed or floating supply is at fault. Then check the alarm diodes (either fixed or floating (to determine which is conducting and caused the alarm.

   Now, remove or disconnect all boards except A18 and the power supply one at a time until the board with the problem is found.

   Lastly, troubleshoot the faulty board.

P/O A18 REGULATOR BOARD Ø8160-66518

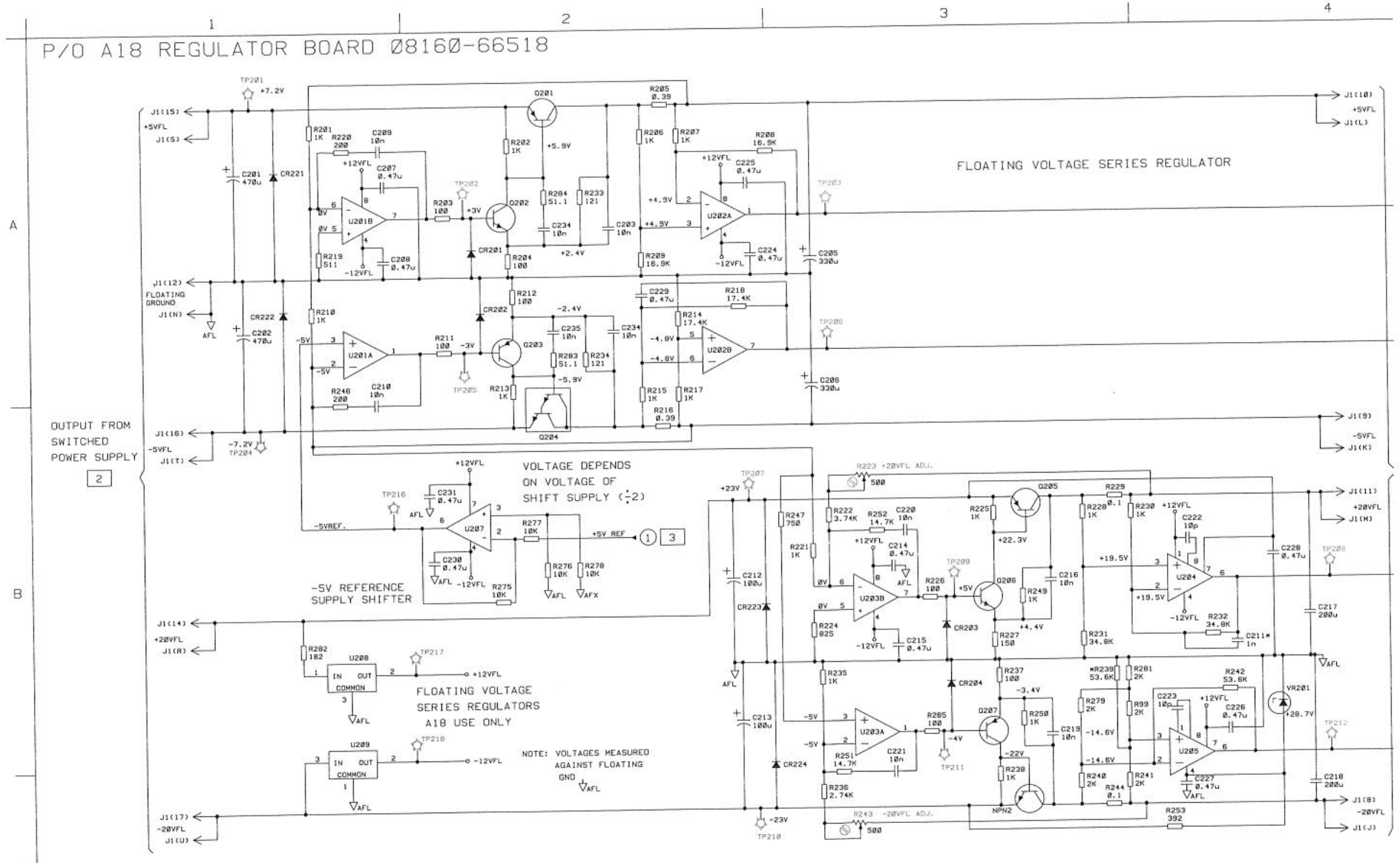


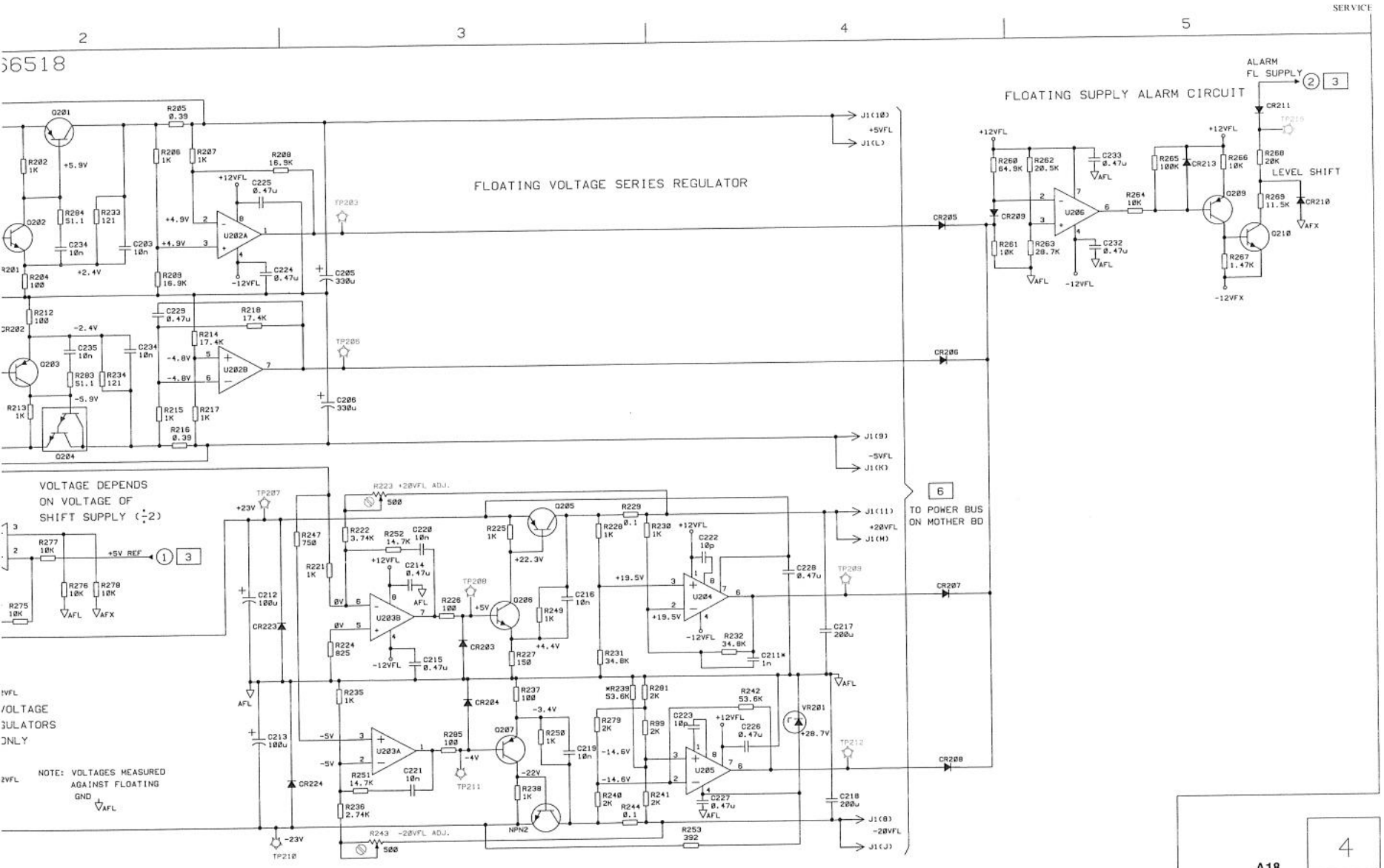

FIXED VOLTAGE SERIES REGULATOR
OVERLOAD ALARM CIRCUIT (FXD AND FL)
FXD SUPPLY ALARM CIRCUIT
ALARM FL SUPPLY
ALARM LED
FOR TROUBLESHOOTING PURPOSE Q12 IS ON SOCKET
+5V REFERENCE SUPPLY
TO POWER BUS ON MOTHER BD
NOTE: VOLTAGES MEASURED AGAINST FIXED GND
J1(5) FILTERED +5V
J1(E)
J1(4) +5VFX
J1(D)
J1(2) -5VFX
J1(B)
J1(3) -5V FILTERED
J1(6) +20VFX
J1(F)
J1(1) -20VFX
J1(A)
R80 +20V FXD ADJ.
R71 -20V FXD ADJ.
+5V REFERENCE
TO R2 (U18/5)
+5V REF
REF. ADJ

A18

3

P/O A18 REGULATOR BOARD Ø816Ø-66518




2
3
4
5
66518
FLOATING VOLTAGE SERIES REGULATOR
FLOATING SUPPLY ALARM CIRCUIT
ALARM
FL SUPPLY
LEVEL SHIFT
TO POWER BUS
ON MOTHER BD
VOLTAGE DEPENDS
ON VOLTAGE OF
SHIFT SUPPLY (÷2)
NOTE: VOLTAGES MEASURED
AGAINST FLOATING
GND
Q201
Q202
Q203
Q204
Q205
Q206
Q207
Q208
Q209
Q210
U202A
U202B
U203B
U203A
U204
U205
U206
VR201
CR201
CR202
CR203
CR204
CR205
CR206
CR207
CR208
CR209
CR210
CR211
CR213
CR223
CR224
TP203
TP206
TP207
TP208
TP209
TP210
TP211
TP212
TP213
TP219
NPN2
R202 1K
R205 0.39
R206 1K
R207 1K
R208 16.9K
R209 16.9K
R212 100
R213 1K
R214 17.4K
R215 1K
R216 0.39
R217 1K
R218 17.4K
R221 1K
R222 3.74K
R223 +20VFL ADJ. 500
R224 825
R225 1K
R226 100
R227 150
R228 1K
R229
R230 1K
R231 34.8K
R232 34.8K
R235 1K
R236 2.74K
R237 100
R238 1K
R239 53.6K
R243 -20VFL ADJ. 500
R244 0.1
R247 750
R249 1K
R250 1K
R251 14.7K
R252 14.7K
R253 392
R260 64.9K
R261 10K
R262 20.5K
R263 28.7K
R264 10K
R265 100K
R266 10K
R267 1.47K
R268 20K
R269 11.5K
R276 10K
R277 10K
R278 10K
R279 2K
R99 2K
R240 2K
R241 2K
R242 53.6K
C201 100u
C202 100u
C203 10n
C205 330u
C206 330u
C211* 1n
C212 100u
C213 100u
C214 0.47u
C215 0.47u
C216 10n
C217 200u
C218 200u
C219 10n
C220 10n
C221 10n
C222 10p
C223 10p
C225 0.47u
C226 0.47u
C227 0.47u
C228 0.47u
C229 0.47u
C232 0.47u
C233 0.47u
C234 10n
C235 10n
+5.9V
+2.4V
-2.4V
-5.9V
+4.9V
-4.8V
+12VFL
-12VFL
+5VFL
-5VFL
+20VFL
-20VFL
+5V REF
+23V
-23V
+22.3V
+19.5V
+4.4V
-3.4V
-4V
-22V
-14.6V
+28.7V
-12VFX
AFL
AFX
J1(10)
J1(L)
J1(9)
J1(K)
J1(11)
J1(M)
J1(8)
J1(J)
6
1 3
2 3
4 3
5 3

SB 4 CONTROLLER

CONTENTS

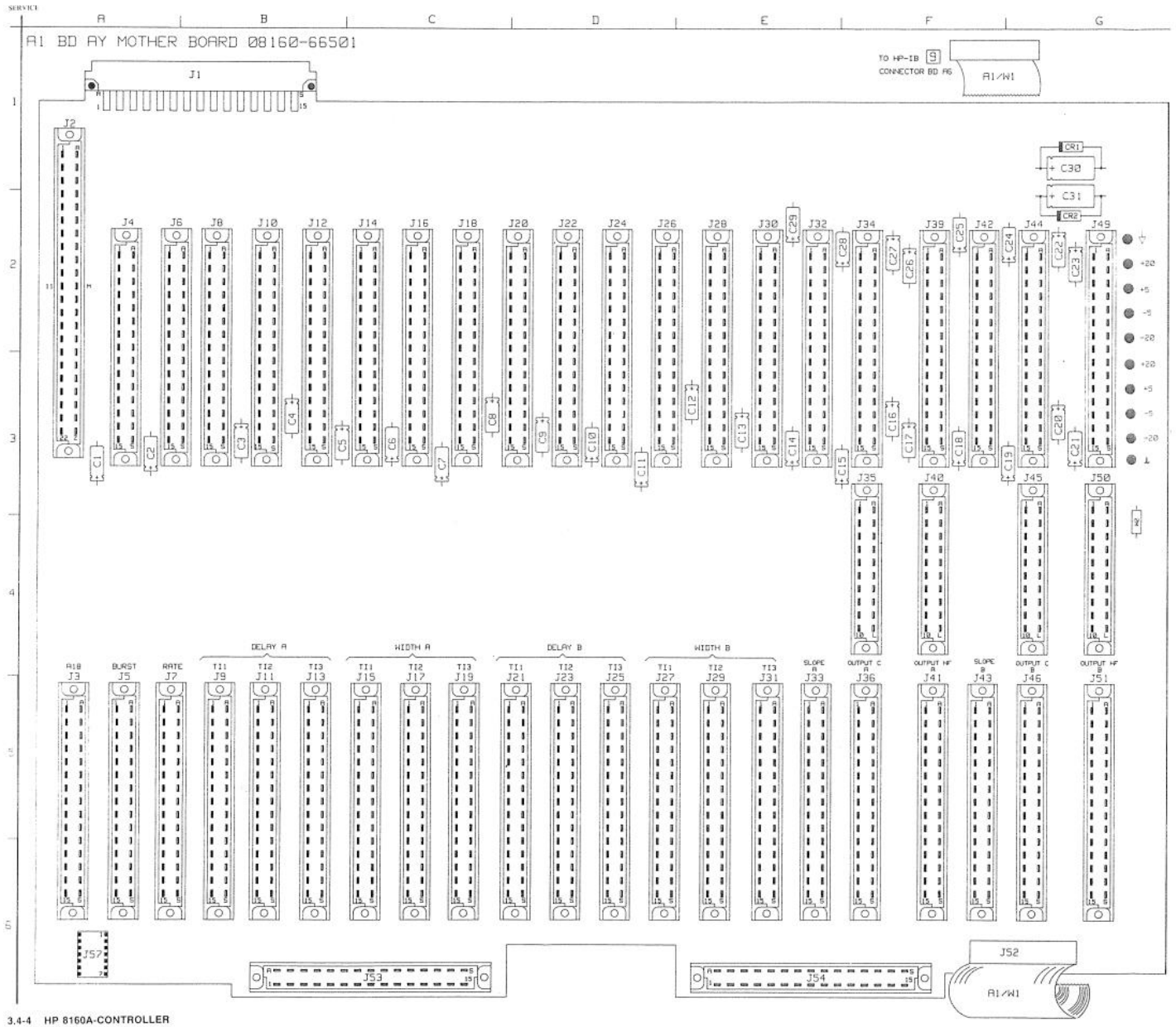
ASSEMBLIES

A1, Motherboard (Main)
A2, Microprocessor (MPU, uP)

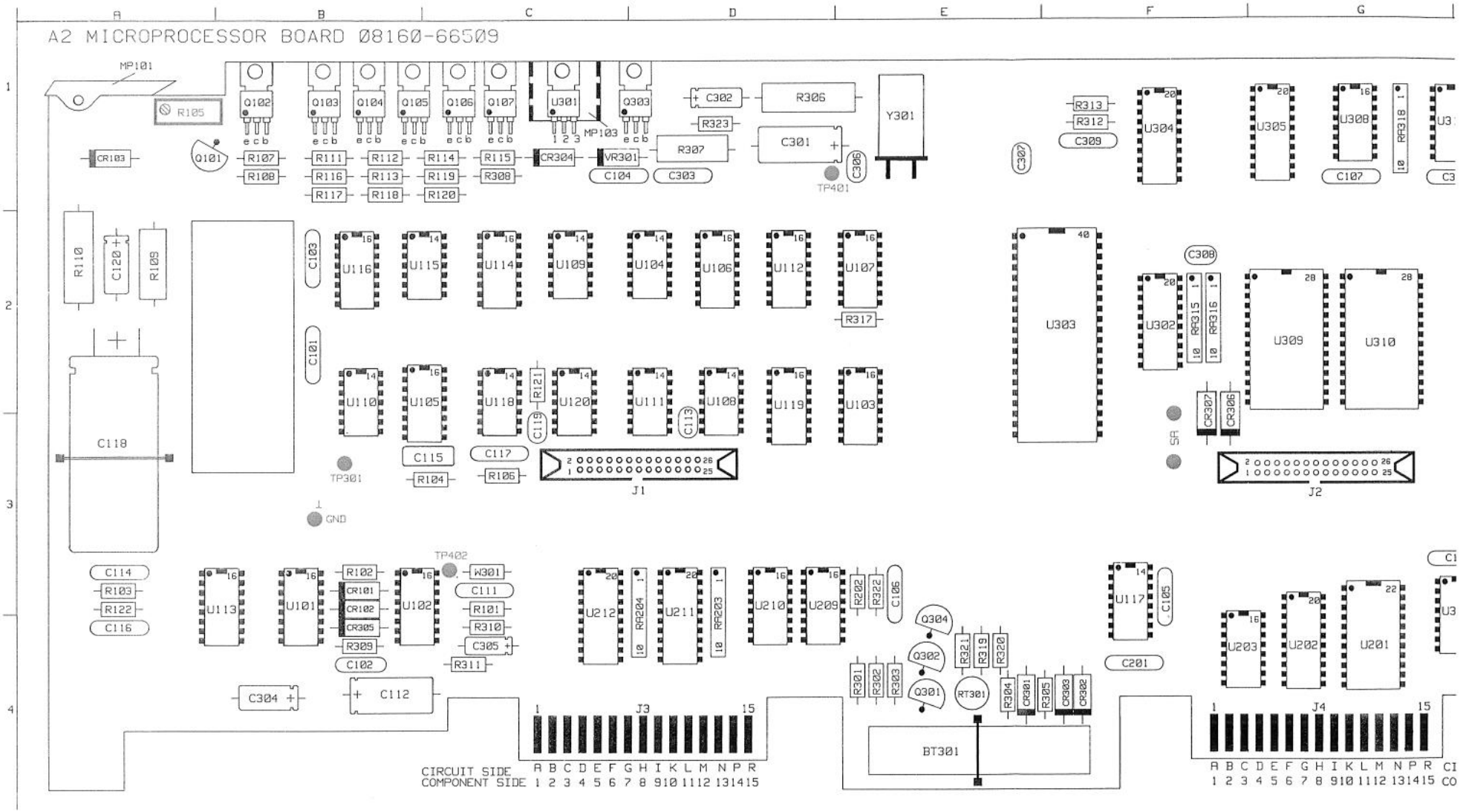
COMPONENT LAYOUT DIAGRAMS

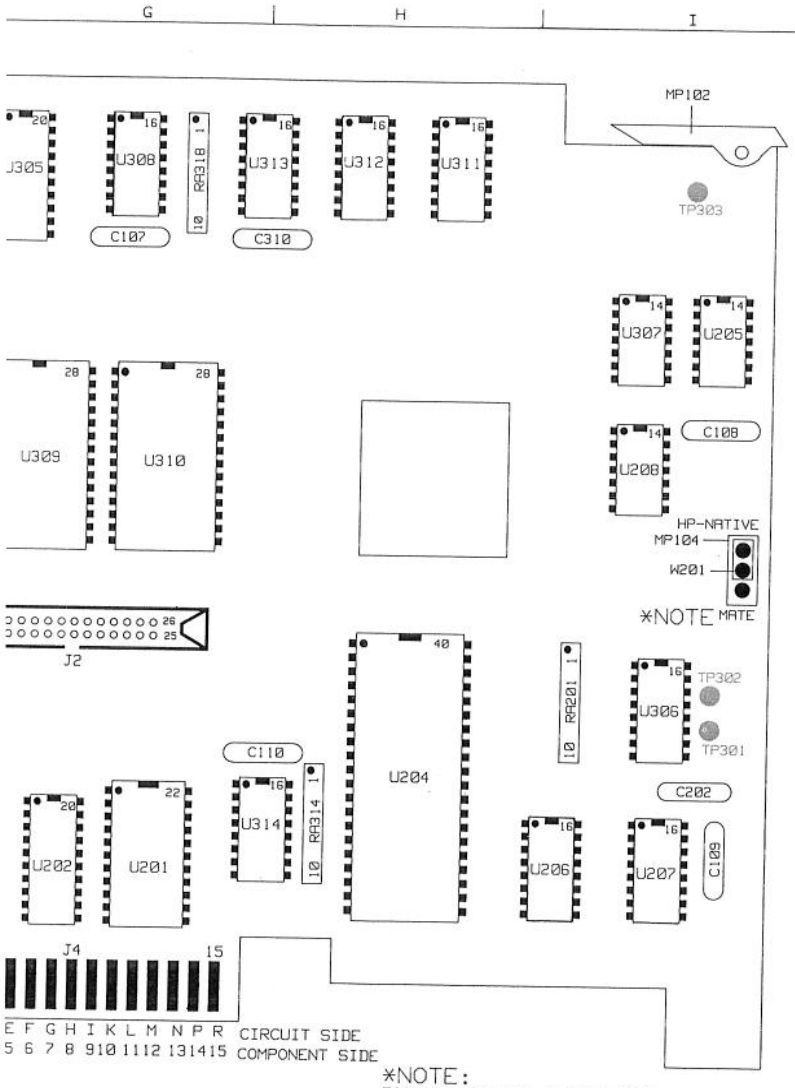
SCHEMATIC DIAGRAMS

TABLE

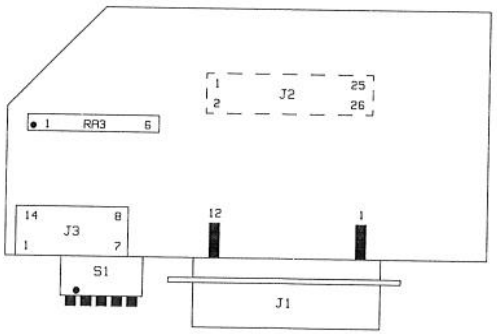


REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
C1	A3	J23	D5
C2	A2	J24	D2
C3	B3	J25	D5
C4	B3	J26	D2
C5	B3	J27	D5
C6	C3	J28	E2
C7	C3	J29	E5
C8	C3	J30	E2
C9	D3	J31	E5
C10	D3	J32	E2
C11	D3	J33	E5
C12	E3	J34	F2
C13	E3	J35	F3
C14	E3	J36	F5
C15	F3	J39	F2
C16	F3	J40	F3
C17	F3	J41	F5
C18	F3	J42	F2
C19	G3	J43	F5
C20	G3	J44	G2
C21	G3	J45	G3
C22	G2	J46	G5
C23	G2	J49	G2
C24	G2	J50	G3
C25	F2	J51	G5
C26	F2	J53	B/C6
C27	F2	J54	E/F6
C28	E2	J57	A6
C29	E2		
C30	G1	W1	F/G6
C31	G2		
CR1	G1/2		
CR2	G1/2		
J1	A/B1		
J2	A1		
J3	A5		
J4	A2		
J5	A5		
J6	A2		
J7	A5		
J8	B2		
J9	B5		
J10	B2		
J11	B5		
J12	B2		
J13	B5		
J14	C2		
J15	C5		
J16	C2		
J17	C5		
J18	C2		
J19	C5		
J20	D2		
J21	D5		
J22	D2		


A2 MICROPROCESSOR BOARD Ø8160-66509
MP101
MP103
R105
Q101
Q102
Q103
Q104
Q105
Q106
Q107
U301
Q303
C302
R306
R323
R307
C301
Y301
R313
R312
C309
U304
U305
U308
RA318
CR103
R107
R108
R111
R116
R117
R112
R113
R118
R114
R119
R120
R115
R308
CR304
VR301
C104
C303
C306
C307
TP401
R110
C120
R109
C103
C101
U116
U115
U114
U109
U104
U106
U112
U107
R317
U303
C308
U302
RA315
RA316
U309
U310
C118
U110
U105
U118
R121
C119
U120
U111
C113
U108
U119
U103
CR307
CR306
SR
TP301
C115
R104
C117
R106
J1
J2
GND
C114
R103
R122
C116
TP402
U113
U101
R102
CR101
CR102
CR305
R309
C102
U102
W301
C111
R101
R310
C305
R311
C304
C112
U212
RA204
U211
RA203
U210
U209
R202
R322
C106
Q304
Q302
Q301
R321
R319
R320
RT301
R304
CR301
R305
CR303
CR302
R301
R302
R303
U117
C105
C201
U203
U202
U201
J3
J4
BT301
CIRCUIT SIDE
COMPONENT SIDE
A B C D E F G H I K L M N P R
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15



A6 BD AY HP-IB (08160-66516)



REF. DES.	GRID LOC.
BT301	E/F4
C101	B2
C102	B4
C103	B2
C104	C1
C105	F3
C106	E3
C107	G1
C108	I2
C109	I4
C110	G/H3
C111	C3
C112	B4
C113	D2/3
C114	A3
C115	B3
C116	A4
C117	C3
C118	A2/3
C119	C3
C120	A2
C201	F4
C202	I3
C301	D1
C302	D1
C303	D1
C304	B4
C305	C4
C306	E1
C307	E1
C308	F2
C309	F1
C310	G/H1
CR101	B3
CR102	B4
CR103	C4
CR301	E4
CR302	F4
CR303	F4
CR304	C1
CR305	B4
CR306	F2
CR307	F2
J1	C/D3
J2	G3
MP101	A1
MP102	I1
MP103	C1
MP104	I3
Q101	A1
Q102	B1
Q103	B1
Q104	B1
Q105	B1
Q106	C1
Q107	C1
Q301	B2
Q302	E4
Q303	E3
Q304	E3
R101	C3
R102	B3
R103	A3
R104	B3
R105	A1
R106	C3
R107	B1
R108	B1
R109	A2
R110	A2
R111	B1
R112	B1
R113	B1
R114	C1
R115	C1
R116	B1
R117	B1
R118	B1
R119	C1
R120	C1
R121	C2/3
R122	A3
R202	E4
R301	E4
R302	E4
R303	E4
R304	E4
R305	E4
R306	D1
R307	D1
R308	C1
R309	B4
R310	C4
R311	C4
R312	F1
R313	F1
R317	E2
R319	E4
R320	E4
R321	E4
R322	E3
R323	D1
RA201	I3
RA203	D3/4
RA204	D3/4
RA314	H3/4
RA315	F2
RA316	F2
RA318	G1
RT301	E4
TP301	B/I3
TP302	I3
TP303	I1
TP401	D2
TP402	B3
U101	B3/4
U102	B3/4
U103	E2
U104	D2
U105	B2
U106	D2
U107	B1
U108	D2
U109	A2
U110	B2
U111	D2
U112	D2
U113	B3/4
U114	C2
U115	B2
U116	B2
U117	F3
U118	C2
U119	D2
U120	C2
U201	G4
U202	F/G4
U203	F4
U204	H3/4
U205	I2
U206	H/I4
U207	I4
U208	I2/3
U209	D3/4
U210	D3/4
U211	D3/4
U212	C3/4
U301	C1
U302	F2
U303	E/F2
U304	F1
U305	F/G1
U306	I3
U307	I2
U308	G1
U309	G2/3
U310	G2/3
U311	H1
U312	H1
U313	G/H1
U314	G/H4
VR301	C1
W201	I3
W301	C3
Y301	E1

INTRODUCTION

The microprocessor board implements the instrument controller which is composed of the following major circuits:

1. Microprocessor Unit (MPU)
2. Eraseable Programmable Read Only Memory (EPROM)
3. Random Access Memory (RAM)
4. Address Decoder (ADD DCDR)
5. General Purpose Interface Adaptor (GPIA)
6. Control Line and Data Interface (CLD I/F)
7. Keyboard Interface (Keybd I/F)
8. Display Interface (DSP I/F)

CONTROLLER OVERVIEW

The controller generates the internal signals used by the instrument to set up the desired instrument output. The internal signals consist of the following types:

1. Device Bus Control Signals
2. Device Bus Address and Data Signals

This is accomplished by directing the MPU to execute the applicable instructions in the CONTROL PROGRAM which is the set of instructions permanently located in ROM (FIRMWARE).

Programming Modes

There are two MODES of programming controller operation.

1. LOCAL MODE: via the front panel KEYBOARD.
2. REMOTE MODE: by a SYSYEM CONTROLLER via the HP-IB INTERFACE.

Programmable Parameters and Modes

The following instrument PARAMETERS and MODES are set by either mode of operation:

1. PERIOD and WIDTH
2. DELAY and DOUBLE PULSE
3. LEADING EDGE, and TRAILING EDGE
4. HIGH LEVEL, and LOW LEVEL
5. BURST
6. INPUT MODES, and OUTPUT MODES.

Microprocessor (MPU or uP)

The purpose of the MPU is to execute the instructions programmed in the EPROM. The signals associated with this activity can be grouped into three busses.

1. An eight bit, bi-directional DATA BUS.
2. A sixteen bit, uni-directional ADDRESS BUS.
3. A CONTROL BUS which is not a true bus; however, these control signals are commonly referred to as a bus.

The MPU has an internal oscillator which is connected to an external crystal.

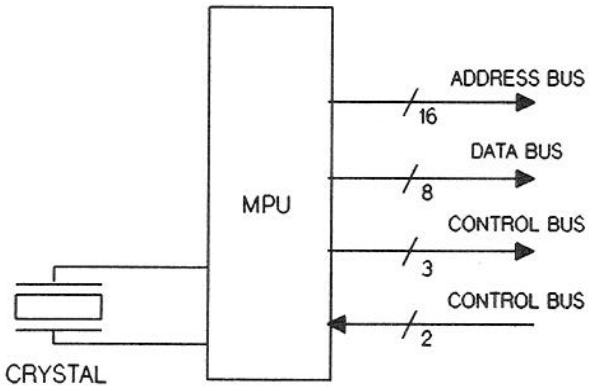


FIGURE 1. MPU Input/Output.

Eraseable Programmable Read only Memory (EPROM)

The EPROM is a random access memory device that can be read; it cannot be written to. Data can be read by addressing a memory location and enabling the EPROM. The data in the EPROM is installed by Hewlett Packard.

Random Access Memory (RAM)

The RAM is a random access memory device that can be read from and written to. Read or write operations are performed by addressing a memory location and enabling the RAM.

Data written into a memory location replaces the previous data. When power is removed from the RAM the data is lost.

However, this instrument has a batteryback-up circuit which provides power to the RAM when the line power is removed.

Address Decoder (ADD DCDR)

The addresses decoded by these devices provide enable signals for the following devices:

1. ROM and RAM
2. GPIA
3. Control Line and Data Interface
4. Keyboard and Display
5. Buffer A2/U306.

General Purpose Interface Adapter (GPIA)

The GPIA is the interface electronics.

The GPIA signal assignment can be divided into the following two groups:

1. Control lines
2. A bi-directional, eight bit data bus.

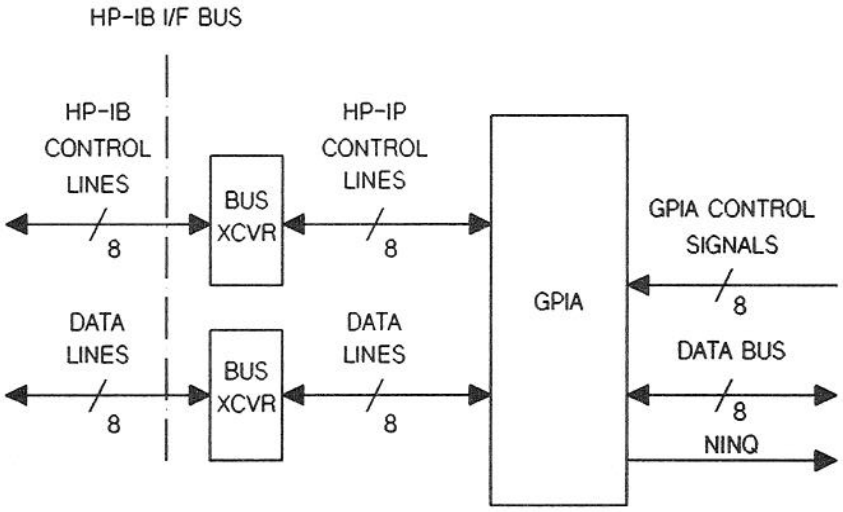


FIGURE 2. GPIA Input/Output Lines.

Control Line and Data Bus Interface (CLD I/F)

This circuit translates the CONTROLLER DATA BUS into:

1. Device Bus address/data signals
2. Device Bus control signals
3. Display signals.

CONTROLLER THEORY

The microprocessor is the main element of the controller and is supported by an EPROM, a RAM, and a GPIA. The microprocessor is:

1. A TTL compatible HMOS device
2. An eight bit parallel processor, capable of addressing sixty-four k-bytes of memory.
3. It has an on chip oscillator.
4. Requires only one +5 Volt supply.

Data Bus

The MPU data bus (**D0-D7**) is an eight bit bi-directional bus. It is the communication link between the MPU and the memory and interface elements.

Address Bus

The MPU address bus (**A0-A15**) is a sixteen bit uni-directional bus. It is used for both addressing and enabling devices.

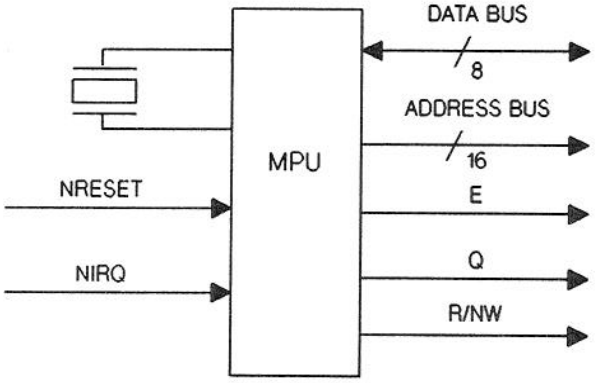


FIGURE 3. MPU Data, Address and Control Lines.

E, Q, R/W(not)

The MPU control signals E, Q, and R/$\overline{W}$ are generated by the MPU to control the flow of data.

The R/$\overline{W}$ (Read/$\overline{\text{Write}}$) line designates whether the MPU is in the read or write mode for each cycle. Thus, it indicates the direction of the data transfer on the data bus.

R/$\overline{W}$ is buffered by (U306B) and then directly used to control the data bus buffer (U302) and the GPIA (U204).

It is also inverted by U208D and then NANDed with E at U208C which is used to control the RAM (U310).

R/$\overline{W}$ is valid on the rising edge of Q. Signals E and Q are Quadrature clock signals where Q leads E. Data is latched on the falling edge of E.

E and Q are ORed (U307A) and then used by the EPROM (U309) and the Main Address Decoder (U308) to indicate when data on the address bus is valid.

RESET(not)

The MPU control signal $\overline{\text{RESET}}$, a power up reset, is sent to the MPU to reset it and cause it to perform a restart routine.

IRQ(not)

The $\overline{\text{IRQ}}$ ($\overline{\text{Interrupt request}}$) signal is transmitted to the MPU from the HP-IB interface via the GPIA (U204) or from the local reset switch via Latch (U206). It is a software or hardware reset and is sent to the MPU to interrupt the current routine and cause it to perform a return to Local mode of operation routine.

RAM Battery Backup

The Battery Back-up circuit provides current to the RAM via Q302 when the instrument power is off. The circuit provides charging current to the battery via Q301 and current to the RAM via Q303 when the instrument power is on.

Hewlett-Packard Interface Bus (HP-IB)

HP-IB is an implementation of the IEEE-488(1978) standard. It is an eight bit parallel interface operating in an asynchronous mode. Therefore a three wire handshake is used for each data byte transferred.

Handshake

The handshake signals are DAV, NRFD, and NDAC.

Management Signals

The management signals, IFC, ATN, SRQ, REN, and EOI, determine in which direction the data is transferred.

General Purpose Interface Adapter

The GPIA is the electronic implementation of this interface providing the link between the instrument controller and a system controller.

HP-IB Address Native/CIIL Tessting

During turn-on the MPU samples Buffer (U203) for the HP-IB address and the HP Native/Mate configuration data and writes this data into the HP-IB controller.

Control Line and Data Interface (CLD I/F)

The Control Line and Data Interface translates the Controller Data Bus into:

1. A sixteen bit parallel Device Bus
2. Three Device Bus control lines which are used to control the circuits that generate the output pulse.
3. Five lines which serve display functions.

The Control Line and Data Interface signals are derived from latches U209, U210, U211, and U212 which are clocked by outputs from the Address Decoder.

TROUBLE SHOOTING

If the microprocessor is operating, it is possible to use signature analysis to troubleshoot some of the controller operations.

Preliminary Checks

Check the following level and signals to determine if the microprocessor is operating:

1. Check the address lines for activity.
2. Check +5 Volts at TP401.
3. Check the **RESET** signal at TP402.
4. Check the E clock at TP301.
5. Check the R/W signal at TP303.

Signature Analysis Set-up

The following steps describe how to set up the instrument for signature analysis:

STEP 1. Set the instrument to the FREE RUN mode of operation.
   a. Switch the instrument OFF.
   b. Short the two SA test pins together.
   c. Switch the instrument ON.
   d. Momentarily SHORT TP402 **(RESET)** to ground, MPU-U303(1).

STEP 2. Connect the signature analyzer to the instrument as described in Table 1.

STEP 3. Set the signal analyzer controls as described in Table 1.

STEP 4. Probe the desired node and compare the signature with Table 1.

SA Tables

Table 1 contains the signatures, signature anzlyzer settings, and connections.

SA Abbreviations

The following abbreviations are used in the signature listings:

1. SH = High Level Signature if the probe is connected to +5 volts
2. SL = Low Level Signature if the probe is connected to ground.
3. SHB = High Level Signature displayed and the probe is blinking.
4. SLB = Low Level Signature displayed and the probe is blinking.

Signature Validity

The EPROM (U309) signatures are valid for HP 8160As with firmware Part Number 08160-82905/-82906.

RAM AND GPIA, SA Exceptions

The RAM (U310) and the GPIA (U204) cannot be tested with signature analysis; thus, if all other signatures are correct, suspect these components.

Display, SA Exceptions

Display trouble shooting procedure: see Service Block 5.

TABLE 1. SIGNATURES

1. Signature Analyzer Settings and connections:
   a. Mode = normal
   b. Start = TTL level, connect to A2 TP303 (A15)
   c. Stop = TTL level, connect to A4 TP303 (A15)
   d. Clock = TTL level, connect to A4 E
   e. Gnd = , , connect to GND.

2. Free-run procedure:
   a. A2 to Service Position
   b. HP 8160A: A2W201 = NATIVE or MATE
   c. Short to A2 SA
   d. Reset by shorting 'notRESET' to GND momentarily.

3. A2/U302, 303, 304, 305, AND 309.
   a. Start = pos
   b. Stop = neg
   c. Clock = neg
   d. SH = 755U

A2/U302:

PIN	NATIVE	MATE
1	SH	SH
2	F9P2	**FP30**
3	F5C5	**4266**
4	1A93	**7H41**
5	7UF0	**9813**
6	1PAC	**9987**
7	H6A6	**5175**
8	A4C5	**A367**
9	3U95	**H846**
10	SL	SL
11	SL	SL
12	SH	SH
13	SL	SL
14	SH	SH
15	SH	SH
16	SH	SH
17	SH	SH
18	SH	SH
19	SHB	SSB
20	SH	SH

A2/U303:

PIN	NATIVE	MATE
1	SL	SL
2	SH	SH
3	SH	SH
4	SH	SH
5	SL	SL
6	SL	SL
7	SH	SH
8	5555	5555
9	CCCC	CCCC
10	7F7F	7F7F
11	5H21	5H21
12	OAFA	OAFA
13	UPFA	UPFA
14	52F8	52F8
15	HC89	HC89
16	2H70	2H70
17	HPPO	HPPO
18	1293	1293
19	HAP7	HAP7
20	3C96	3C96
21	3827	3827
22	755U	755U
23	SHB	SHB
24	SL	SL
25	SH	SH
26	SL	SL
27	SH	SH
28	SH	SH
29	SH	SH
30	SH	SH
31	SH	SH
32	SH	SH
33	SH	SH
34	SLB	SLB
35	SLB	SLB
36	SH	SH
37	SH	SH
38	SLB	SLB
39	SHB	SHB
40	SH	SH

A2/U304:

PIN	NATIVE	MATE
1	SH	SH
2	5555	5555
3	CCCC	CCCC
4	7F7F	7F7F
5	5H21	5H21
6	OAFA	OAFA
7	UPFH	UPFH
8	52F8	52F8
9	HC89	HC89
10	SL	SL
11	HC89	HC89
12	52F8	52F8
13	UPFH	UPFH
14	OAFA	OAFA
15	5H21	5H21
16	7F7F	7F7F
17	CCCC	CCCC
18	5555	5555
19	SL	SL
20	SH	SH

A2/U305:

PIN	NATIVE	MATE
1	SH	SH
2	7707	7707
3	577A	577A
4	HH86	HH86
5	89F1	89F1
6	AC99	AC99
7	PCF3	PCF3
8	1180	1180
9	755U	755U
10	SL	SL
11	755U	755U
12	1180	1180
13	PCF3	PCF3
14	AC99	AC99
15	89F1	89F1
16	HH86	HH86
17	577A	577A
18	7707	7707
19	SL	SL
20	SH	SH

A2/U309:

PIN	NATIVE	MATE
1	SH	SH
2	3C96	3C96
3	HC89	HC89
4	52F8	52F8
5	UPFH	UPFH
6	OAFA	OAFA
7	5H21	5H21
8	7F7F	7F7F
9	CCCC	CCCC
10	5555	5555
11	F9P2	**FP30**
12	F5C5	**4266**
13	1A93	**7H41**
14	SL	SL
15	7UFO	**9813**
16	1PAC	**9978**
17	H6A6	**5175**
18	A4C5	**A367**
19	3U95	**HA46**
20	SLB	SLB
21	1293	1293
22	SL	SL
23	HAP7	HAP7
24	HPPO	HPPO
25	2H70	2H70
26	3827	3827
27	755U	755U
28	SH	SH

4. A2/U308
   a. Start = positive
   b. Stop = negative
   c. Clock = positive
   d. SH = 0001

A2/U308:

PIN	NATIVE	MATE
1	4FCA	4FCA
2	4868	4868
3	9UP1	0UP1
4	0002	0002
5	SL	SL
6	SHB	SHB
7	P257	P257
8	SL	SL
9	U3H7	U3H7
10	0994	0994
11	6H4C	6H4C
12	F2A4	F2A4
13	PC03	PC03
14	12U1	12U1
15	4P08	4P08
16	SH	SH

5. A2/U311, 312, 313
   a. Start = positive
   b. Stop = positive
   c. Clock = negative
   d. SH = 0001

A2/U311:

PIN	NATIVE	MATE
1	7791	7791
2	6321	6321
3	6U28	6U28
4	PC03	PC03
5	SL	SL
6	SHB	SHB
7	8F6F	8F6F
8	SL	SL
9	03H6	03H6
10	85UF	85UF
11	5H9A	5H9A
12	058C	058C
13	F183	F183
14	P034	P034
15	98P0	98P0
16	SH	SH

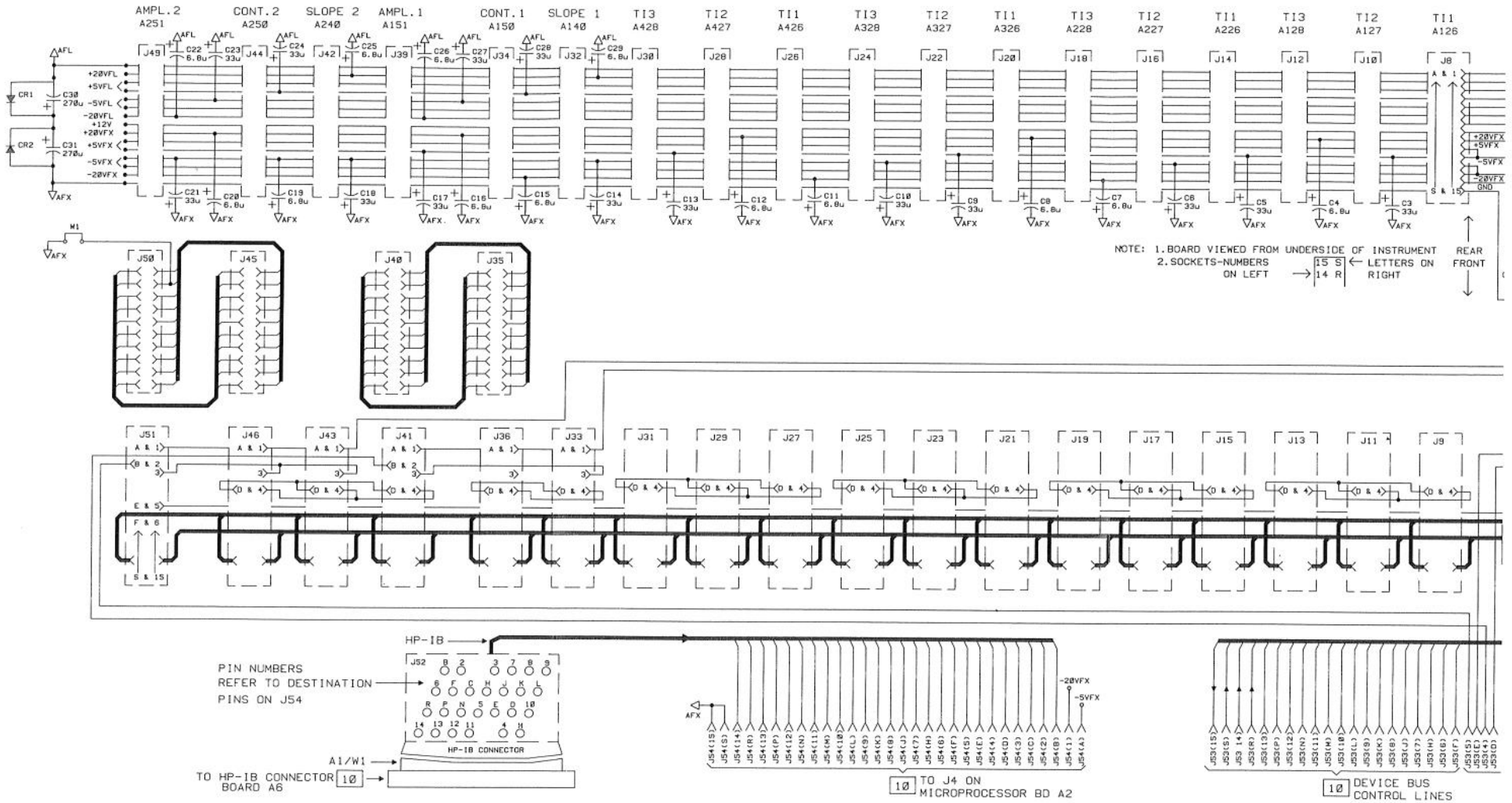
A2/U312:

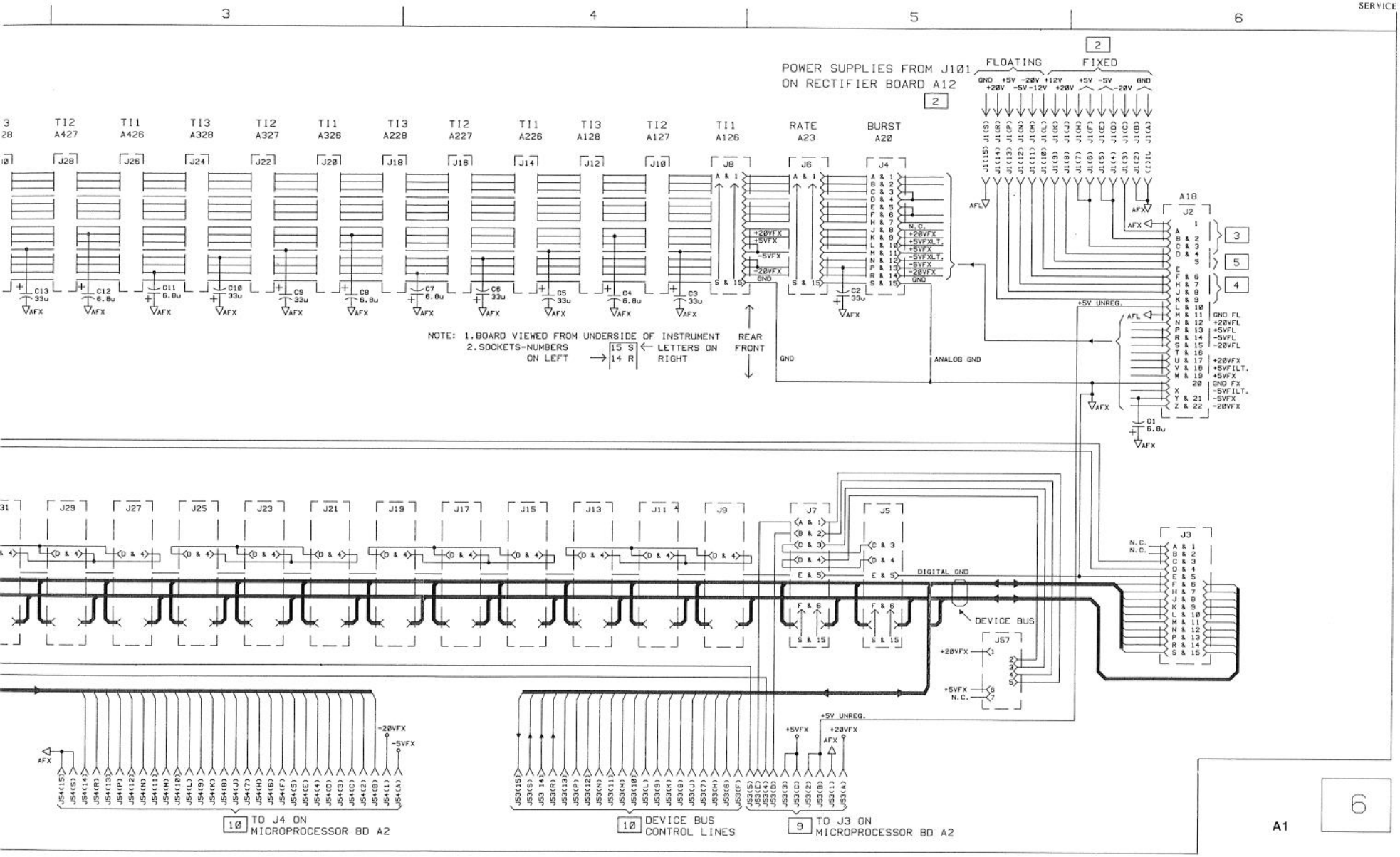
PIN	NATIVE	MATE
1	0994	0994
2	6H4C	6H4C
3	F2A4	F2A4
4	6U28	6U28
5	SL	SL
6	SHB	SHB
7	P00H	P00H
8	SL	SL
9	A3UU	A3UU
10	CA13	CA13
11	SH	SH
12	96FA	96FA
13	SH	SH
14	SH	SH
15	SH	SH
16	SH	SH

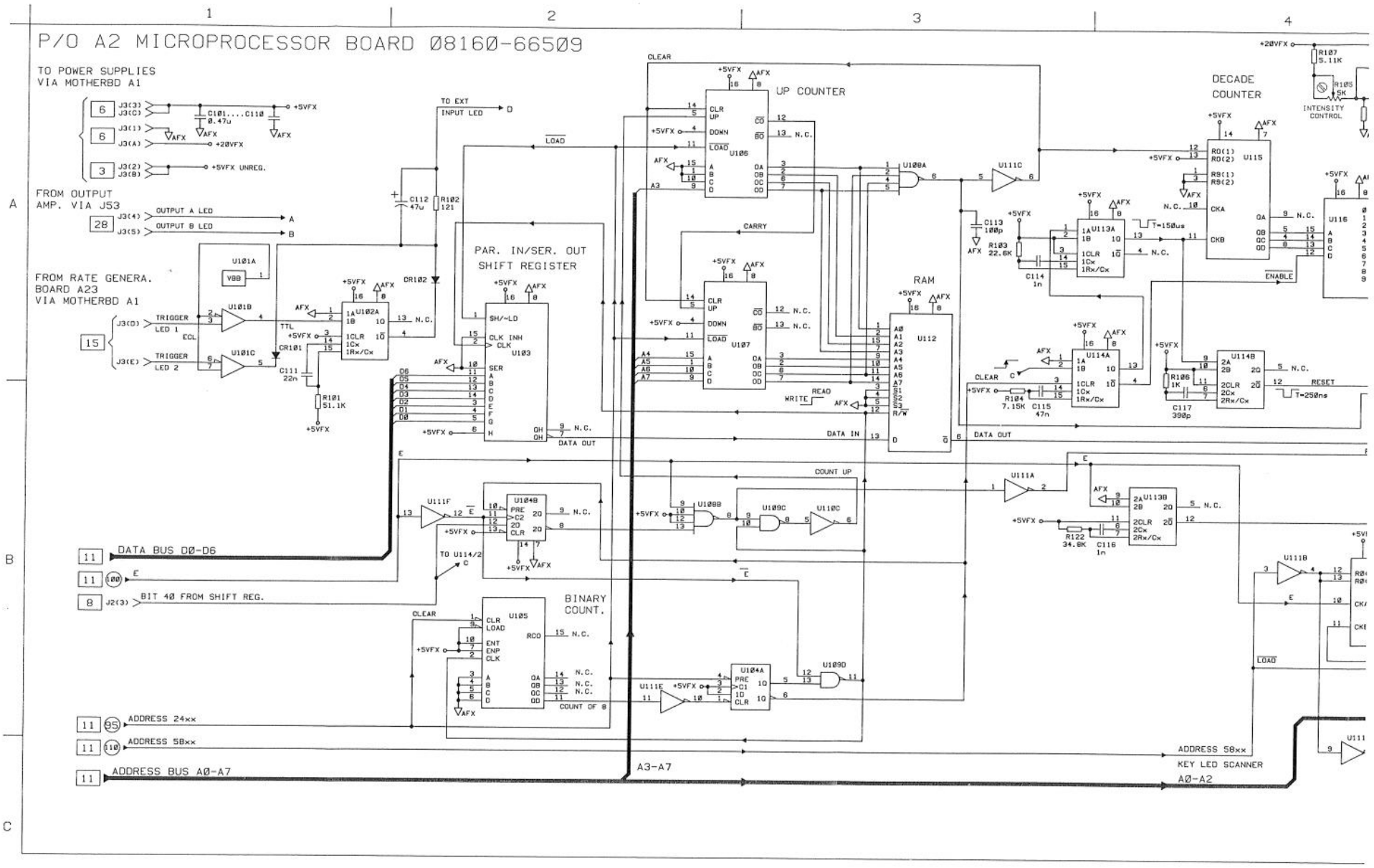
A2/U313:

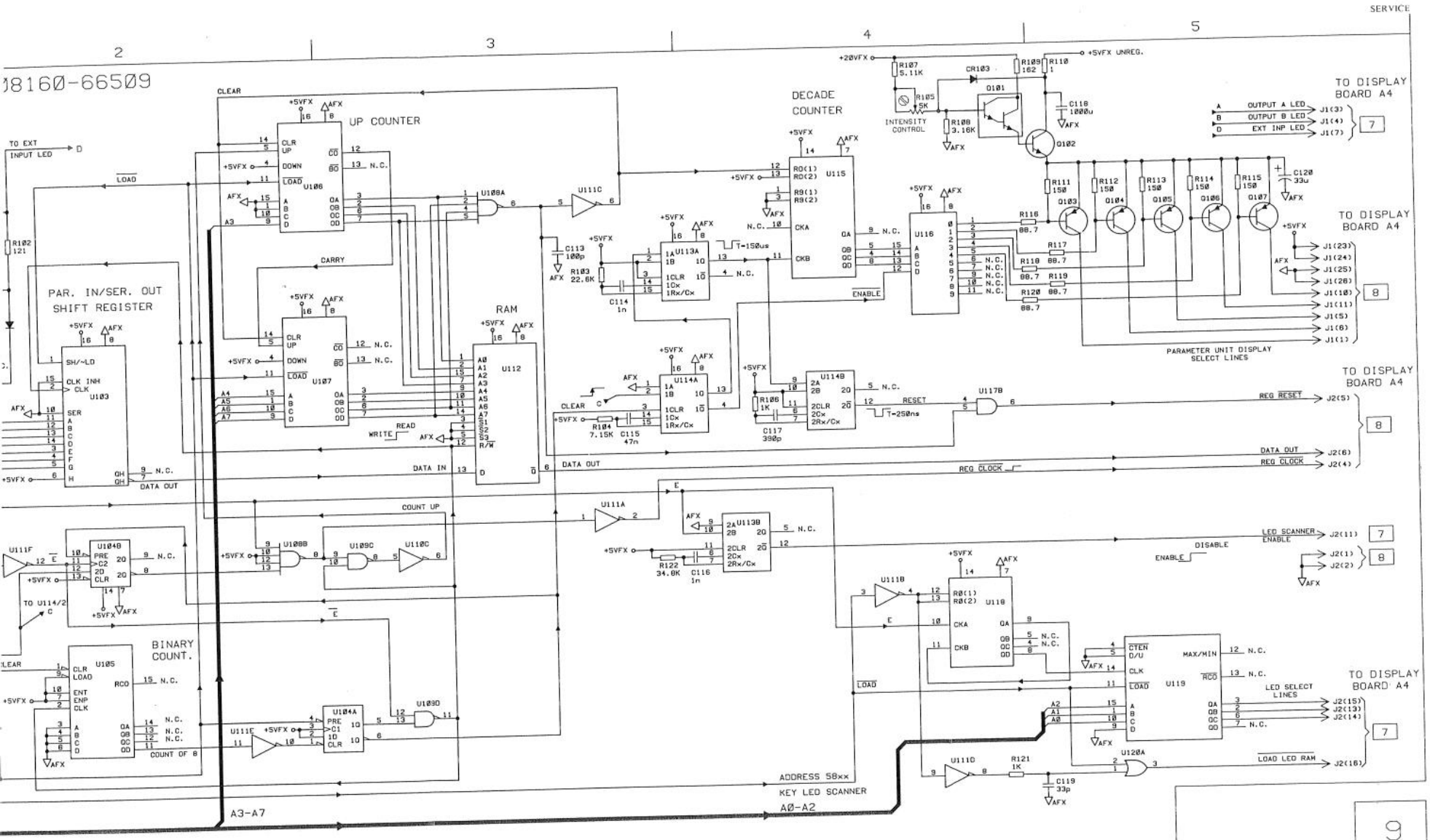
PIN	NATIVE	MATE
1	0994	0994
2	6H4C	6H4C
3	F2A4	F2A4
4	6U2C	6U2C
5	SL	SL
6	SHB	SHB
7	4676	4676
8	SL	SL
9	AA68	AA68
10	H75C	H75C
11	SH	SH
12	546H	546H
13	SH	SH
14	SH	SH
15	SH	SH
16	SH	SH

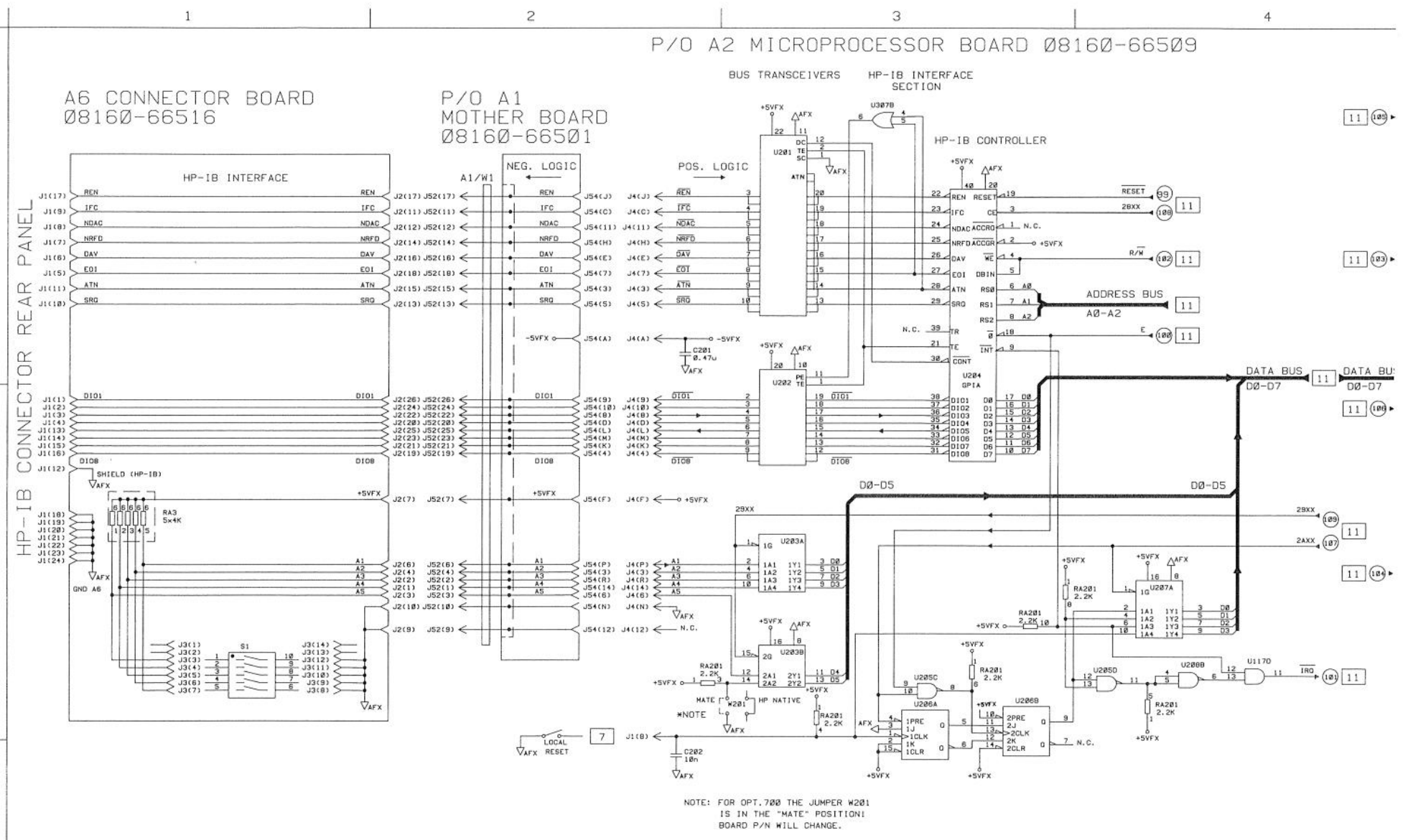
A1 MOTHER BOARD Ø8160-665Ø1

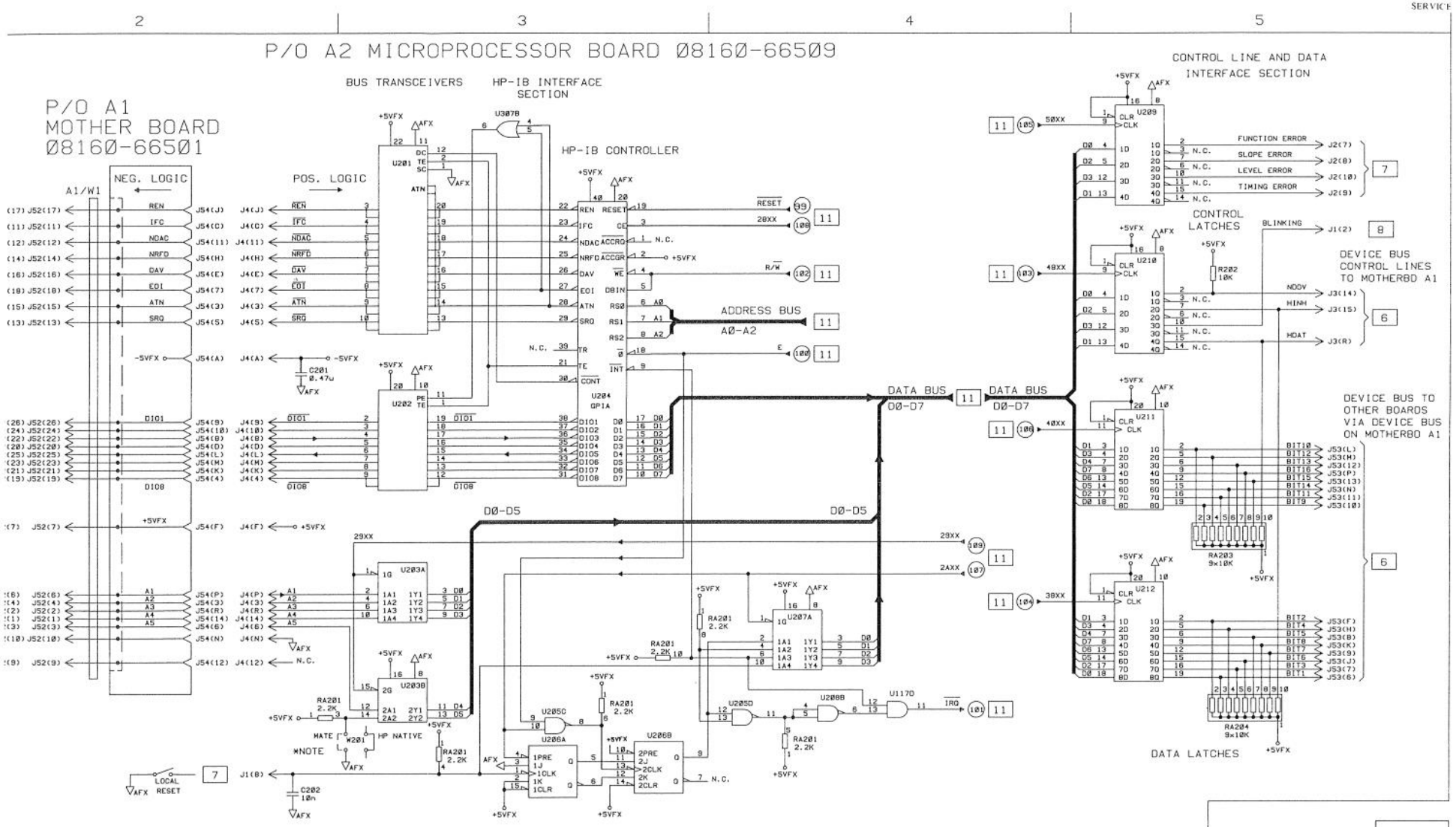


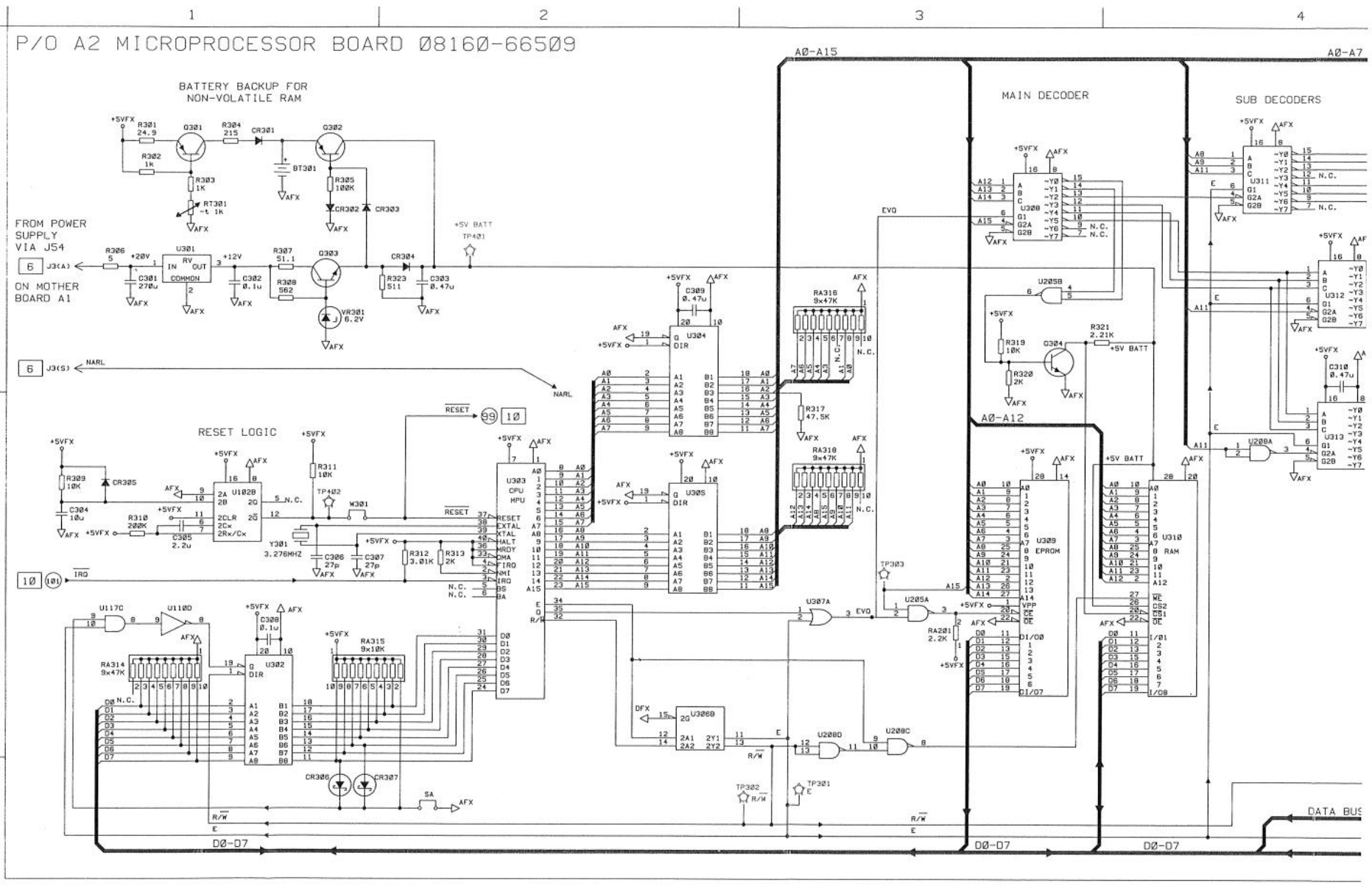

3
4
5
6
2
POWER SUPPLIES FROM J101
ON RECTIFIER BOARD A12
2
FLOATING
FIXED
GND +20V +5V -5V -20V +12V +20V +5V -5V -20V GND
TI2 A427
TI1 A426
TI3 A328
TI2 A327
TI1 A326
TI3 A228
TI2 A227
TI1 A226
TI3 A128
TI2 A127
TI1 A126
RATE A23
BURST A20
J8
J6
J4
A18
J2
+20VFX
+5VFX
-5VFX
-20VFX
GND
N.C.
+5VFXLT.
-5VFXLT.
AFX
AFL
+5V UNREG.
ANALOG GND
GND FL
+20VFL
+5VFL
-5VFL
-20VFL
GND FX
-5VFILT.
+20VFILT.
C1 6.8u
C2 33u
C3 33u
C4 6.8u
C5 33u
C6 33u
C7 6.8u
C8 6.8u
C9 33u
C10 33u
C11 6.8u
C12 6.8u
C13 33u
NOTE: 1. BOARD VIEWED FROM UNDERSIDE OF INSTRUMENT
2. SOCKETS-NUMBERS ON LEFT
15 S
14 R
LETTERS ON RIGHT
REAR
FRONT
J29
J27
J25
J23
J21
J19
J17
J15
J13
J11
J9
J7
J5
J3
DIGITAL GND
DEVICE BUS
J57
+20VFX
+5VFX
N.C.
-20VFX
-5VFX
+5V UNREG.
+5VFX
+20VFX
AFX
J54(15) J54(S) J54(14) J54(R) J54(P) J54(12) J54(N) J54(11) J54(M) J54(10) J54(L) J54(9) J54(K) J54(8) J54(J) J54(7) J54(H) J54(6) J54(F) J54(5) J54(E) J54(4) J54(D) J54(3) J54(C) J54(2) J54(B) J54(1) J54(A)
J53(15) J53(S) J53 14 J53(R) J53(P) J53(13) J53(N) J53(11) J53(M) J53(10) J53(L) J53(9) J53(K) J53(8) J53(J) J53(7) J53(H) J53(6) J53(F) J53(E) J53(5) J53(D) J53(4) J53(C) J53(3) J53(2) J53(B) J53(1) J53(A)
10 TO J4 ON MICROPROCESSOR BD A2
10 DEVICE BUS CONTROL LINES
9 TO J3 ON MICROPROCESSOR BD A2
A1
6

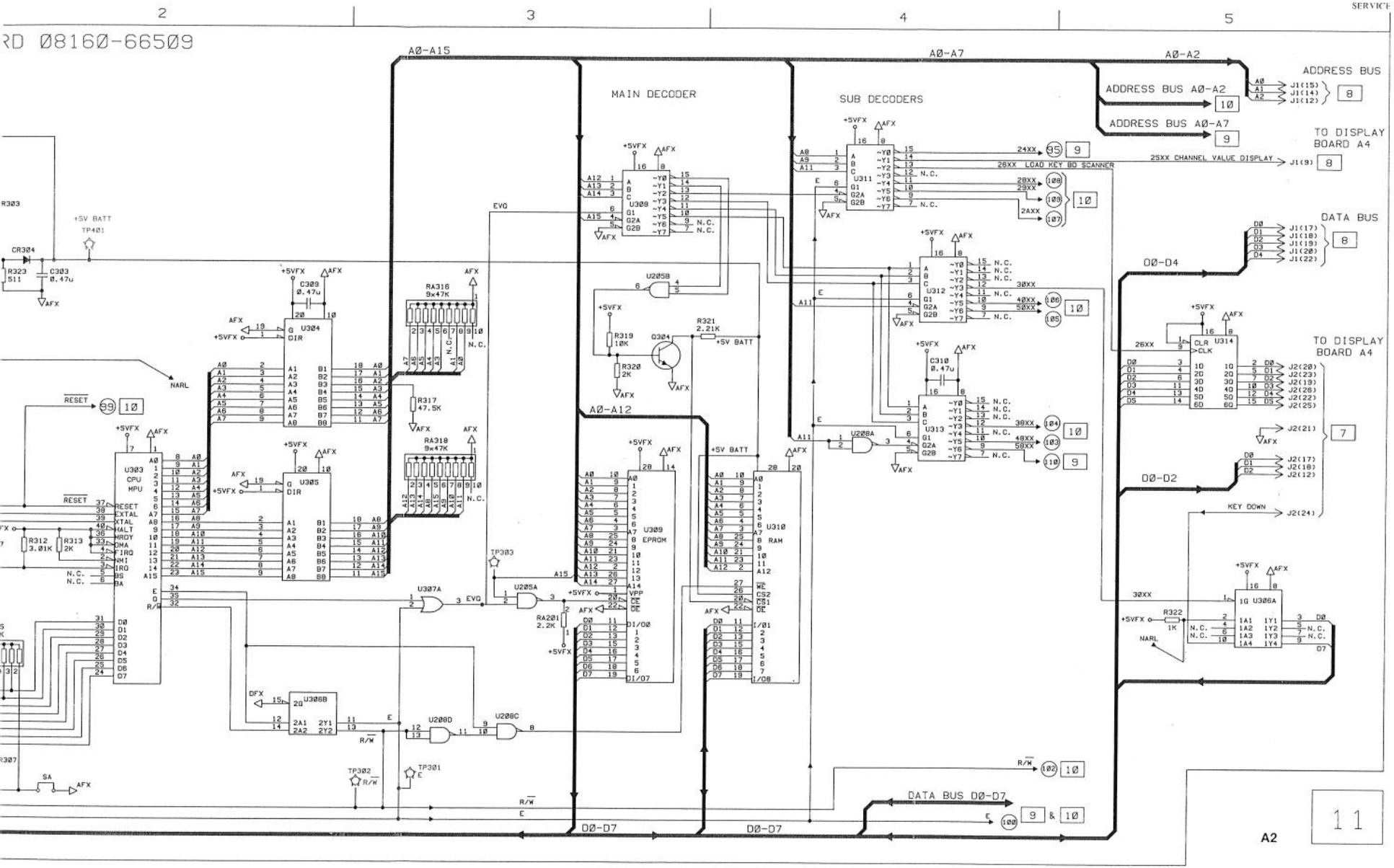

P/O A2 MICROPROCESSOR BOARD Ø8160-66509
TO POWER SUPPLIES VIA MOTHERBD A1
FROM OUTPUT AMP. VIA J53
FROM RATE GENERA. BOARD A23 VIA MOTHERBD A1
TO EXT INPUT LED
PAR. IN/SER. OUT SHIFT REGISTER
UP COUNTER
DECADE COUNTER
RAM
BINARY COUNT.
INTENSITY CONTROL
DATA BUS DØ-D6
BIT 4Ø FROM SHIFT REG.
ADDRESS 24xx
ADDRESS 58xx
ADDRESS BUS AØ-A7
A3-A7
AØ-A2
KEY LED SCANNER


08160-66509
2
3
4
5
UP COUNTER
DECADE COUNTER
RAM
PAR. IN/SER. OUT SHIFT REGISTER
BINARY COUNT.
INTENSITY CONTROL
PARAMETER UNIT DISPLAY SELECT LINES
LED SELECT LINES
TO DISPLAY BOARD A4
TO EXT INPUT LED
OUTPUT A LED
OUTPUT B LED
EXT INP LED
REG RESET
DATA OUT
REG CLOCK
LED SCANNER ENABLE
LOAD LED RAM
ADDRESS 58xx
KEY LED SCANNER
A0-A2
A3-A7
A2
9
HP 8160A-CONTROLLER
3.4-111


P/O A2 MICROPROCESSOR BOARD Ø8160-66509
A6 CONNECTOR BOARD
Ø8160-66516
P/O A1
MOTHER BOARD
Ø8160-66501
HP-IB CONNECTOR REAR PANEL
HP-IB INTERFACE
NEG. LOGIC
POS. LOGIC
A1/W1
BUS TRANSCEIVERS
HP-IB INTERFACE SECTION
HP-IB CONTROLLER
ADDRESS BUS
A0-A2
DATA BUS
D0-D7
D0-D5
SHIELD (HP-IB)
GND A6
RA3
5x4K
S1
LOCAL
RESET
HATE
HP NATIVE
W201
*NOTE
NOTE: FOR OPT.700 THE JUMPER W201
IS IN THE "MATE" POSITION!
BOARD P/N WILL CHANGE.


2
3
4
5
P/O A2 MICROPROCESSOR BOARD Ø8160-66509
BUS TRANSCEIVERS
HP-IB INTERFACE SECTION
CONTROL LINE AND DATA INTERFACE SECTION
P/O A1 MOTHER BOARD Ø8160-66501
A1/W1
NEG. LOGIC
POS. LOGIC
HP-IB CONTROLLER
REN
IFC
NDAC
NRFD
DAV
EOI
ATN
SRQ
-5VFX
+5VFX
DIO1
DIO8
ADDRESS BUS
A0-A2
DATA BUS
D0-D7
CONTROL LATCHES
DEVICE BUS CONTROL LINES TO MOTHERBD A1
DEVICE BUS TO OTHER BOARDS VIA DEVICE BUS ON MOTHERBD A1
DATA LATCHES
FUNCTION ERROR
SLOPE ERROR
LEVEL ERROR
TIMING ERROR
BLINKING
NDDV
HINH
HDAT
RESET
R/W
E
IRQ
LOCAL
MATE
HP NATIVE
*NOTE
NOTE: FOR OPT.700 THE JUMPER W201 IS IN THE "MATE" POSITION! BOARD P/N WILL CHANGE.


P/O A2 MICROPROCESSOR BOARD Ø8160-66509
BATTERY BACKUP FOR NON-VOLATILE RAM
FROM POWER SUPPLY VIA J54
ON MOTHER BOARD A1
RESET LOGIC
MAIN DECODER
SUB DECODERS
A0-A15
A0-A7
A0-A12
EVQ
NARL
RESET
IRQ
DATA BUS
D0-D7
R/W
E
+5V BATT
+5VFX
AFX


2
3
4
5
SERVICE
RD 08160-66509
A0-A15
A0-A7
A0-A2
MAIN DECODER
SUB DECODERS
ADDRESS BUS
ADDRESS BUS A0-A2
ADDRESS BUS A0-A7
TO DISPLAY BOARD A4
DATA BUS
A0-A12
D0-D4
D0-D2
EVQ
NARL
RESET
+5V BATT
+5VFX
AFX
U303 CPU MPU
U304 DIR
U305 DIR
U309 EPROM
U310 RAM
U311
U312
U313
U314
U306A
U306B
U205A
U205B
U207A
U208A
U208C
U208D
R316 9x47K
RA318 9x47K
R317 47.5K
R319 10K
R320 2K
R321 2.21K
R322 1K
R323 511
R312 3.01K
R313 2K
RA201 2.2K
C303 0.47u
C309 0.47u
C310 0.47u
Q304
CR304
TP301
TP302
TP303
TP401
24XX
25XX CHANNEL VALUE DISPLAY
26XX LOAD KEY BD SCANNER
28XX
29XX
2AXX
30XX
40XX
50XX
KEY DOWN
DATA BUS D0-D7
D0-D7
R/W
E
11
A2
HP 8160A-CONTROLLER
3.4-131

SB 5 DISPLAY AND KEYBOARD

CONTENTS

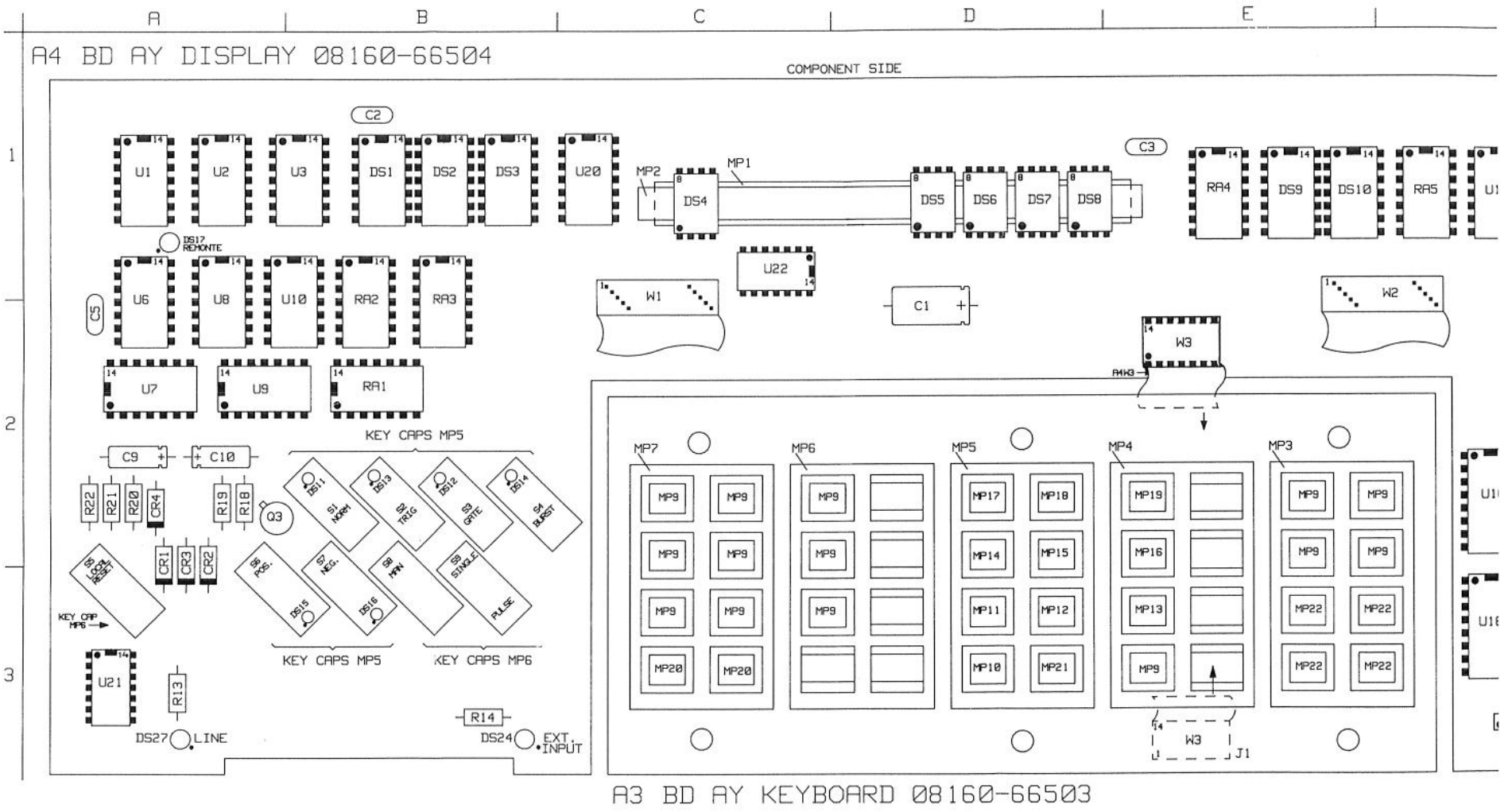
ASSEMBLIES

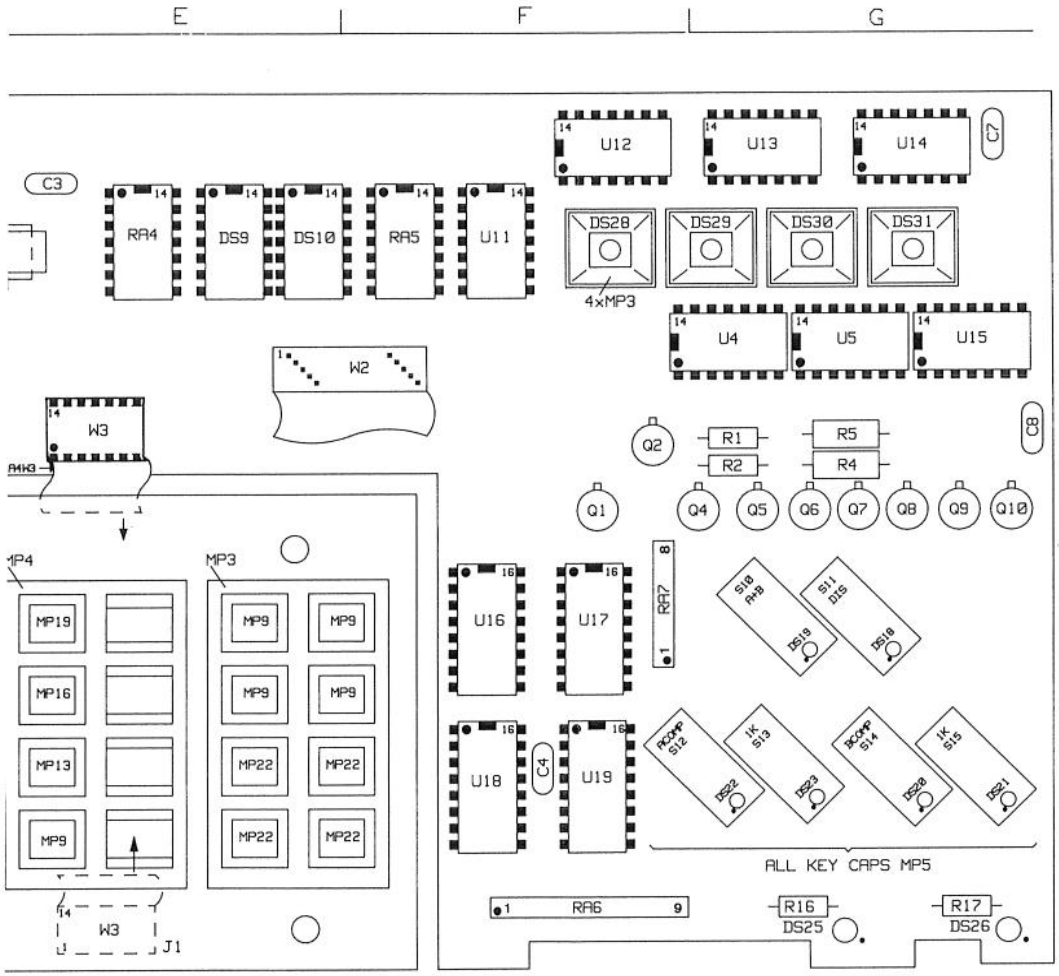
A3, Key Board
A4, Display Board

COMPONENT LAYOUT DIAGRAM

SCHEMATIC DIAGRAMS

FIGURES


A
B
C
D
E
1
2
3
A4 BD AY DISPLAY 08160-66504
COMPONENT SIDE
C2
C3
U1
U2
U3
DS1
DS2
DS3
U20
MP2
MP1
DS4
DS5
DS6
DS7
DS8
RA4
DS9
DS10
RA5
DS17 REMONTE
U6
U8
U10
RA2
RA3
U22
W1
C1
W2
C5
W3
A4K3
U7
U9
RA1
KEY CAPS MP5
C9
C10
R22
R21
R20
CR4
R19
R18
Q3
DS11
S1 NORM
DS13
S2 TRIG
DS12
S3 GATE
DS14
S4 BURST
CR1
CR3
CR2
S5 LOCK RESET
S6 POS.
DS15
S7 NEG.
DS16
S8 MAN
S9 SINGLE
PULSE
KEY CAP MP6
KEY CAPS MP5
KEY CAPS MP6
U21
R13
R14
DS27 LINE
DS24 EXT INPUT
MP7
MP6
MP5
MP4
MP3
MP9
MP20
MP17
MP18
MP14
MP15
MP11
MP12
MP10
MP21
MP19
MP16
MP13
MP22
W3
J1
A3 BD AY KEYBOARD 08160-66503



A3

REF. DES.	GRID LOC.
J1	E3
MP3	E2/3
MP4	E2/3
MP5	D2/3
MP6	C2/3
MP7	C2/3
MP9	C2
MP10	D3
MP11	D3
MP12	D3
MP13	E3
MP14	D2
MP15	D2
MP16	E2
MP17	D2
MP18	D2
MP19	E2
MP20	C3
MP21	D3
MP22	E3

A4

REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
C1	D2	R1	G2	W1	C1/2
C2	B1	R2	G2	W2	F1/2
C3	E1	R4	G2	W3	E2
C4	F3	R5	G2		
C5	A2	R13	A3		
C7	G1	R14	B3		
C8	G2	R15	F3		
C9	A2	R16	G3		
C10	A2	R17	G3		
CR1	A2/3	R18	A3		
CR2	A2/3	R19	A3		
CR3	A2/3	R20	A3		
CR4	A2	R21	A3		
DS1	B1	R22	A3		
DS2	B1	RA1	B2		
DS3	B1	RA2	B1/2		
DS4	C1	RA3	B1/2		
DS5	D1	RA4	E1		
DS6	D1	RA5	F1		
DS7	D1	RA6	F3		
DS8	D1	RA7	F2		
DS9	E1				
DS10	E1	S1	B2		
DS11	B2	S2	B2		
DS12	B2	S3	B2		
DS13	B2	S4	B2		
DS14	B2	S5	B2/3		
DS15	B3	S6	A2/3		
DS16	B3	S7	B2/3		
DS17	A1	S8	B2/3		
DS18	G2	S9	B2/3		
DS19	G2	S10	G2		
DS20	G3	S11	G2		
DS21	G3	S12	F/G3		
DS22	G3	S13	G3		
DS23	G3	S14	G3		
DS24	B3	S15	G3		
DS25	G3	U1	A1		
DS26	G3	U2	A1		
DS27	A3	U3	B1		
DS28	F1	U4	G1		
DS29	G1	U5	G1		
DS30	G1	U6	A1/2		
DS31	G1	U7	A2		
MP1	C1	U8	A1/2		
MP2	C1	U9	A2		
MP3	F1	U10	A1		
MP5	A/B2	U12	F1		
MP6	B3	U13	G1		
Q1	F2	U14	G1		
Q2	F2	U15	G1		
Q3	A2	U16	F2		
Q4	G2	U17	F2		
Q5	G2	U18	F3		
Q6	G2	U19	F3		
Q7	G2	U20	C1		
Q8	G2	U21	A3		
Q9	G2	U22	C1		
Q10	G2				

INTRODUCTION

The display contains the following sections:

1. Parameter and Unit
2. Channel and Value
3. Error
4. Key LEDS
5. Blink Generetor

The keyboard contains the keypad and scanning circuitry.

DISPLAY BOARD (A4)

Parameter and Unit

The Parameter display consists of three 5x7 dot matrix displays and the Unit display consists of two 5x7 dot matrix displays.

The microprocessor writes 7 bits of column display data to the Parallel In/Serial Out Shift Register A2/U103 and Input H of the register is connected to +5 V.

Thus, the register outputs 8 bits of serial data to RAM A2/U112 which is addressed by Up-Counter A2/U106 and U107.

This procedure of shifting 8 bits through to the RAM is repeated until 200 bits of data are written into the RAM.

The 25 data bits associated with input H of the shift register will not be used for display purposes. However, every 40th bit will be used as a detect signal.

Up-Counter A2/U106 and U107 is now cleared and begins addressing the RAM again. The column display data is read from the RAM and clocked into Parameter and Unit display shift register A4/U5-1.

At every 40th cycle, the display shift register contains data for five columns (one column of each display).

Also, at this 40th cycle, a 'bit 40 detect' circuit A2/U104B,U108, and U111 stops the shift register clock and turns on a column register enabling transistor, A2/Q103,4,5,6, or 7.

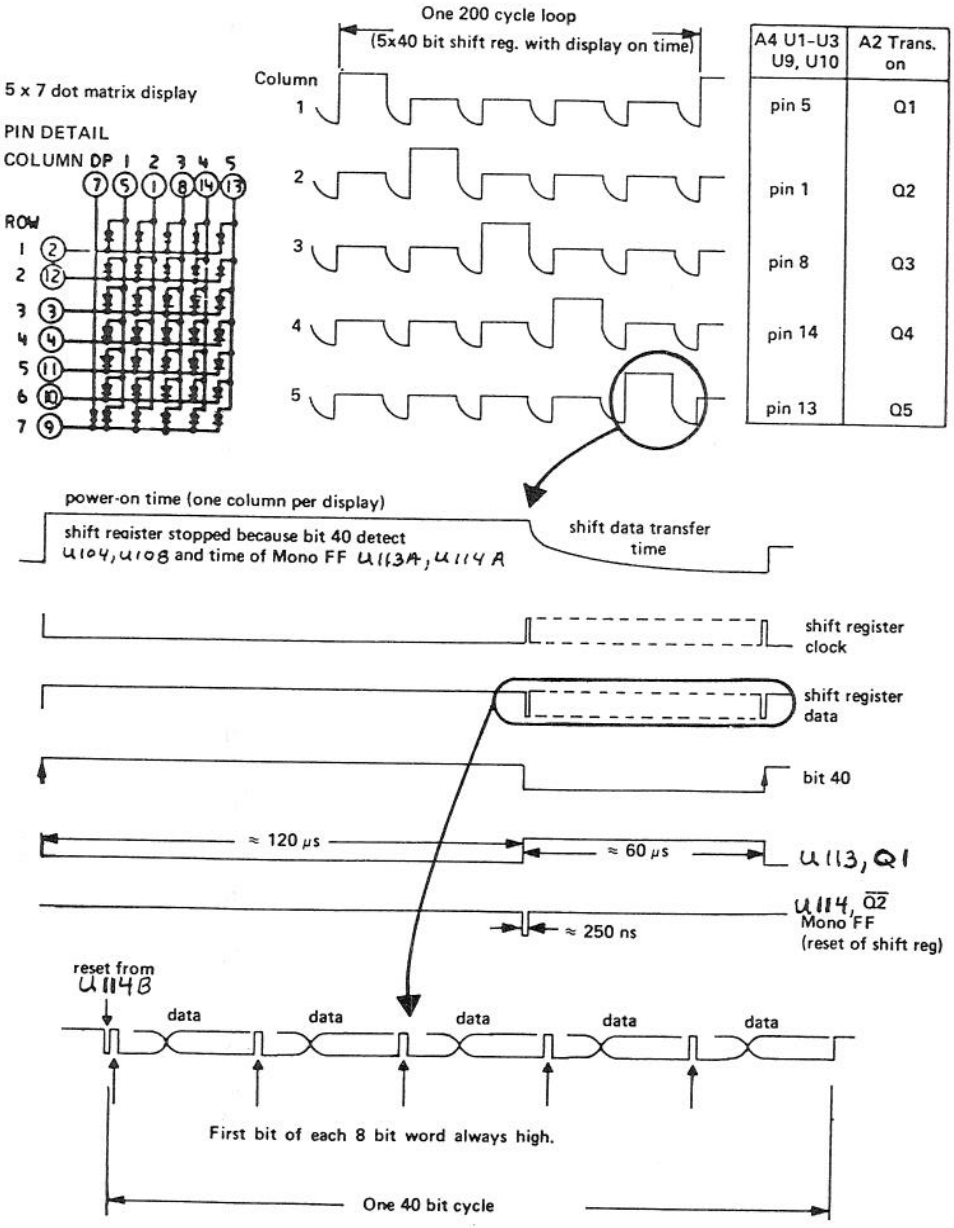
Now, the column data in the shift registers are valid and the corresponding columns in each display are enabled. This turns on the required LEDs in each display.

The reading procedure repeats for bits 41-80, 81-120, 121-160, and 161-200 of the RAM data. The reading sequences is repeated until the display data is updated. Then, the write sequence is performed again.

Transistors A2/Q103-7 are controlled by monostable circuit A2/U113A and U114A, decade counter A2/U115, and converter A2/U116.

After the time constant of monostable circuit A2/U113A and U114A, monostable circuit A2/U114B is started which clears the display shift register. Then, the next 40 bits can be shifted into the register.

FIGURE 1. Parameter/Unit Display Timing Cycle.



CHANNEL AND VALUE

The Channel display consists of one 5x7 dot matrix display.

The Value display consists of four 5x7 dot matrix displays.

The display includes decoder, driver, and memory circuits.

Display information is output on the data bus to the displays which are in a parallel conficuration.

The correct display is selected via decoder A4/U20 which decodes address lines A0, A1, and A2.

The decoder is selected by sub-decoder A2/U311.

ERROR DISPLAY

The 4 error indicators each use a single +5 V incandescent lamp.

Error data is latched from the data bus by A2/U404 which controls drivers A4/U15a-d.

The drivers are connected to the error lamps A4/DS28-31.

BLINK GENERATOR

The Parameter display will blink when a parameter is selected and when certain errors occur.

The blinking generator is enabled by the signal 'blinking'. This signal is output by the microprocessor on the data bus and latched into the device bus by A2/U405.

When enabled, the generator circuit switches A4/Q3 on and off which changes the logic level at the dot matrix drivers A4/U6-10. The coulumns are enabled in the normal manner.

KEY AND REMOTE LEDS

The key LEDs and the REMOTE LED are arranged in a 2x7 matrix.

The microprocessor outputs data to RAM A4/U17.

The RAM addresses and WE(not) come from KEY LED scanner A2/U119.

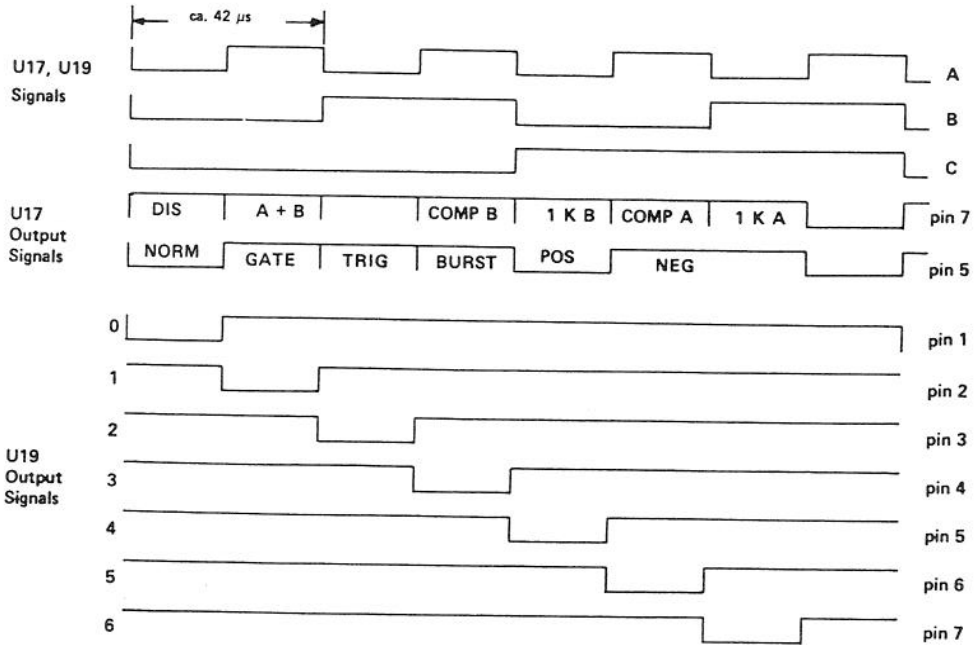
Pin 2 of the RAM is connected to ground. Thus, the RAM is always enabled.

Data is written into the RAM when WE(not) is low and complementary data is read out to the LED matrix when WE(not) is high.

The RAM outputs, pins 5 and 7, turn transistors Q1 and Q2 off which enables row 1 or row 2 fo the LED matrix.

The address lines are decoded by A4/U19 to enable the columns of the matrix by successively turning A4/Q10-4 on.

FIGURE 2. Key LED Timing Cycle.



A LED is on when U17 and U19 outputs are of low coincidence.
U19 will be disabled via Mono-FF A2 U113 when E fails.

KEYBOARD

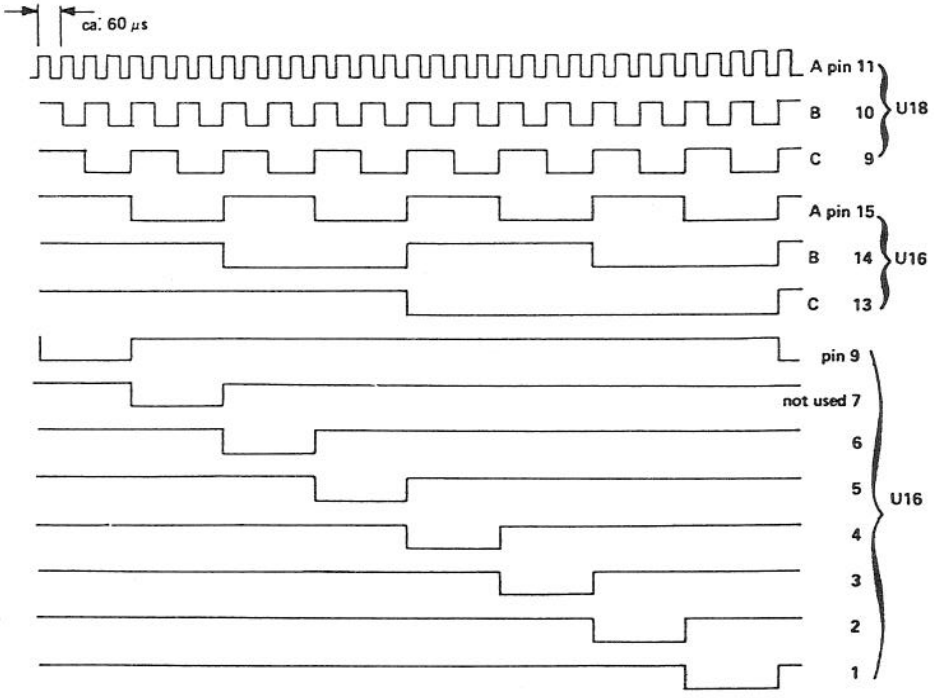
The keyboard is arranged into an 8 x 7 matrix.

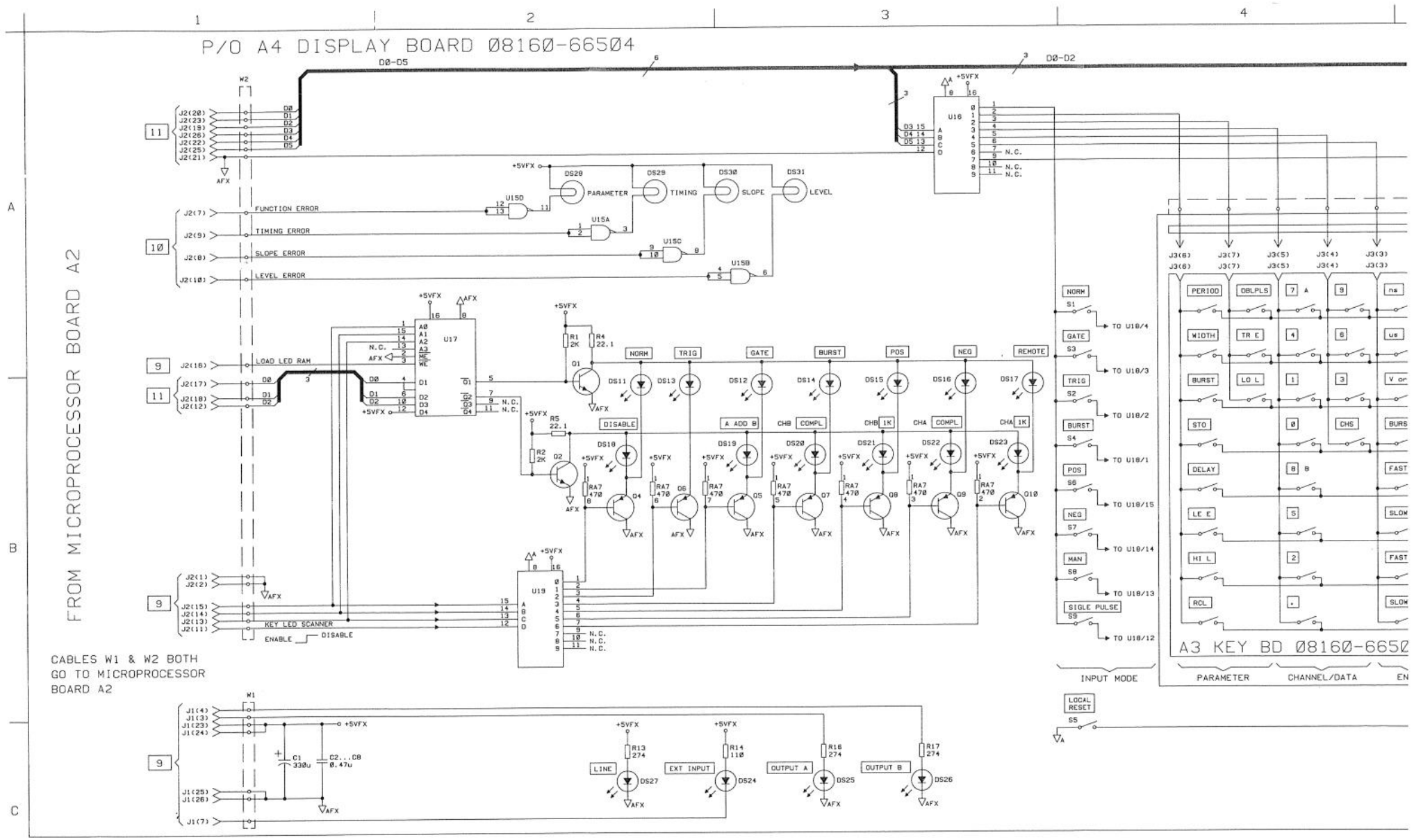
A4/U16 decodes data bus lines D3-5 and strobes the columns of the matrix.

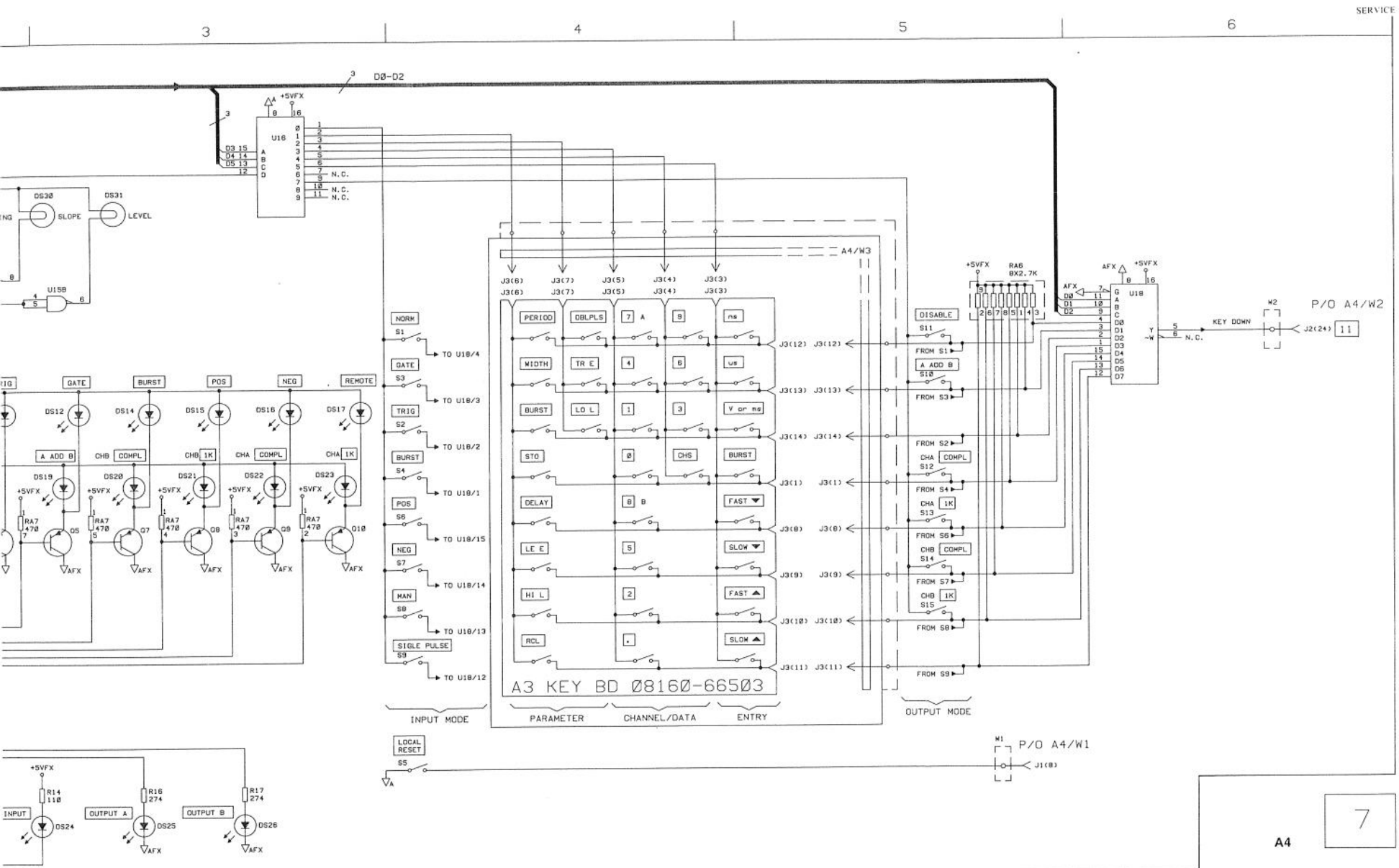
A4/U18 is a 3 to 1 multiplexer. It decodes data bus lines D0-2 and scans the rows of the matrix.

The strobing and scanning detects a closed key switch and returns the information to the MPU via A4/U18 output 'y' which is the Key Down signal.

FIGURE 3. Keyboard Scanner Timing Cycle.



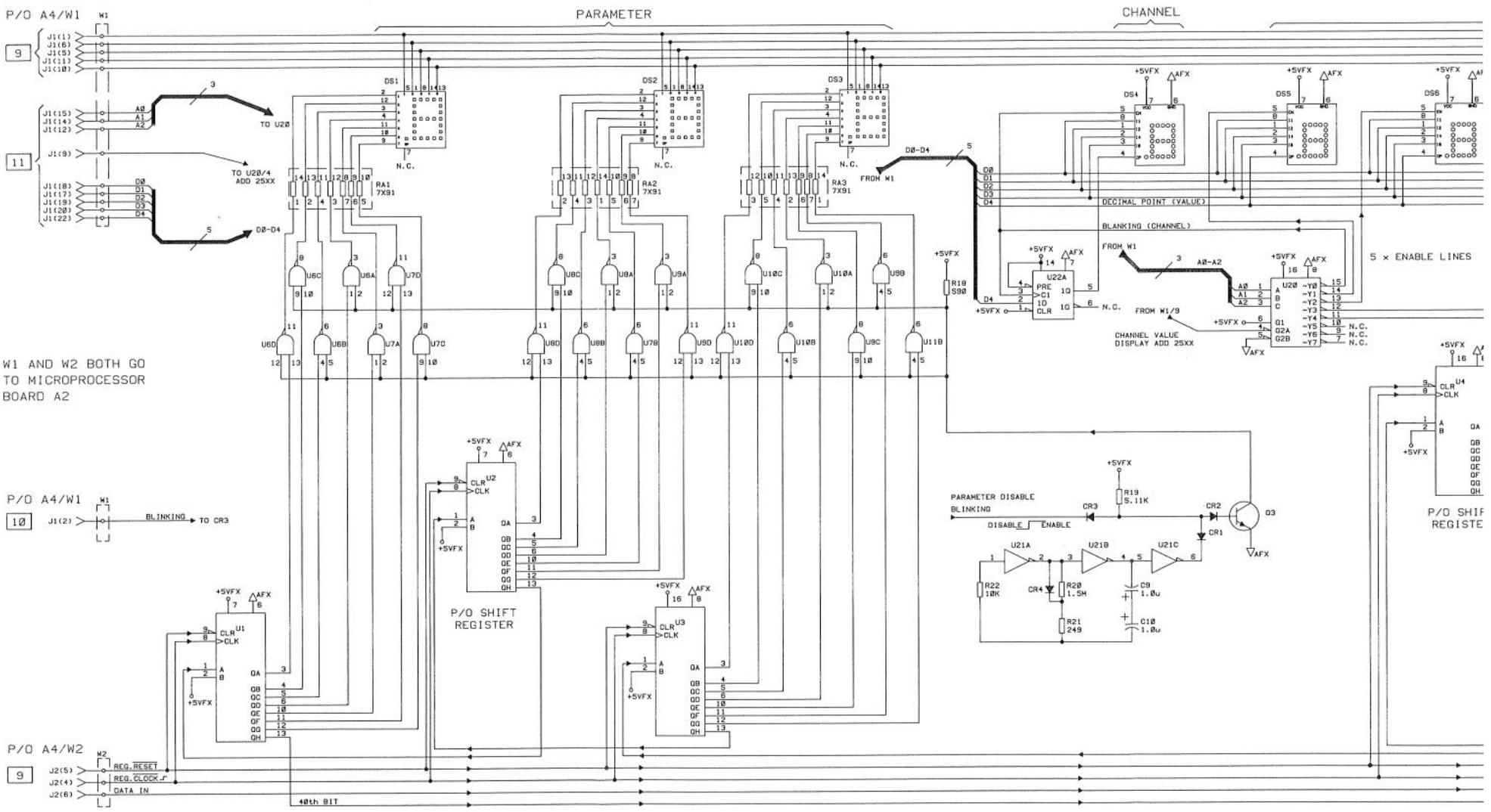

P/O A4 DISPLAY BOARD 08160-66504
FROM MICROPROCESSOR BOARD A2
D0-D5
D0-D2
W2
W1
FUNCTION ERROR
TIMING ERROR
SLOPE ERROR
LEVEL ERROR
LOAD LED RAM
KEY LED SCANNER
ENABLE
DISABLE
PARAMETER
TIMING
SLOPE
LEVEL
NORM
TRIG
GATE
BURST
POS
NEG
REMOTE
DISABLE
A ADD B
CHB
COMPL
CHB
1K
CHA
COMPL
CHA
1K
LINE
EXT INPUT
OUTPUT A
OUTPUT B
NORM
GATE
TRIG
BURST
POS
NEG
MAN
SIGLE PULSE
LOCAL RESET
TO U10/4
TO U10/3
TO U10/2
TO U10/1
TO U10/15
TO U10/14
TO U10/13
TO U10/12
PER10D
DBLPLS
WIDTH
TR E
BURST
LO L
STO
DELAY
LE E
HI L
RCL
A3 KEY BD 08160-6650
INPUT MODE
PARAMETER
CHANNEL/DATA
CABLES W1 & W2 BOTH
GO TO MICROPROCESSOR
BOARD A2

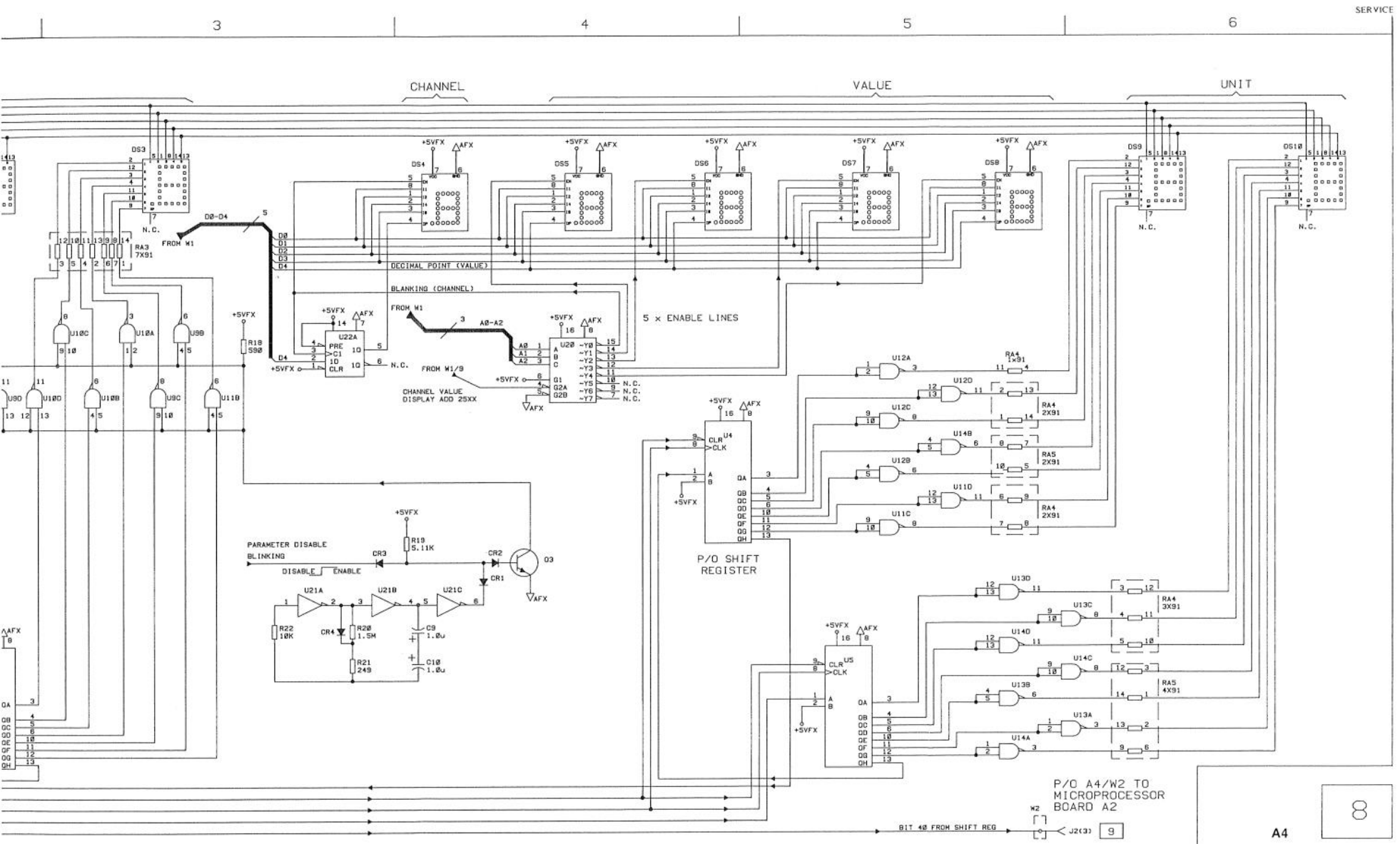

3
4
5
6
D0-D2
+5VFX
U16
D3 15
D4 14
D5 13
12
N.C.
N.C.
N.C.
DS30
SLOPE
DS31
LEVEL
U15B
A4/W3
J3(6)
J3(7)
J3(5)
J3(4)
J3(3)
NORM
S1
TO U18/4
GATE
S3
TO U18/3
TRIG
S2
TO U18/2
BURST
S4
TO U18/1
POS
S6
TO U18/15
NEG
S7
TO U18/14
MAN
S8
TO U18/13
SIGLE PULSE
S9
TO U18/12
PERIOD
OBLPLS
WIDTH
TR E
BURST
LO L
STO
DELAY
LE E
HI L
RCL
7 A
8 B
9
4
5
6
1
2
3
0
.
ns
us
V or ns
CHS
FAST
SLOW
FAST
SLOW
A3 KEY BD 08160-66503
INPUT MODE
PARAMETER
CHANNEL/DATA
ENTRY
OUTPUT MODE
DISABLE
S11
FROM S1
A ADD B
S10
FROM S3
FROM S2
CHA COMPL
S12
FROM S4
CHA 1K
S13
FROM S6
CHB COMPL
S14
FROM S7
CHB 1K
S15
FROM S8
FROM S9
RA6
8X2.7K
U18
KEY DOWN
N.C.
M2
P/O A4/W2
J2(24)
11
LOCAL RESET
S5
M1
P/O A4/W1
J1(8)
GATE
BURST
POS
NEG
REMOTE
A ADD B
CHB COMPL
CHB 1K
CHA COMPL
CHA 1K
DS12
DS14
DS15
DS16
DS17
DS19
DS20
DS21
DS22
DS23
RA7
470
Q5
Q7
Q8
Q9
Q10
AFX
INPUT
OUTPUT A
OUTPUT B
R14
110
R16
274
R17
274
DS24
DS25
DS26

A4

7

P/O A4 DISPLAY BOARD 08160-65004




3
4
5
6
CHANNEL
VALUE
UNIT
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
N.C.
RA3
7X91
D0-D4
FROM W1
DECIMAL POINT (VALUE)
BLANKING (CHANNEL)
5 x ENABLE LINES
A0-A2
CHANNEL VALUE
DISPLAY ADD 25XX
U22A
U20
U10C
U10A
U9B
U9D
U10D
U10B
U9C
U11B
R18
590
PARAMETER DISABLE
BLINKING
DISABLE
ENABLE
CR3
CR2
CR1
Q3
R19
5.11K
U21A
U21B
U21C
R22
10K
CR4
R20
1.5M
R21
249
C9
1.0u
C10
1.0u
U4
U5
P/O SHIFT
REGISTER
U12A
U12D
U12C
U14B
U12B
U11D
U11C
U13D
U13C
U14D
U14C
U13B
U13A
U14A
RA4
1X91
RA4
2X91
RA5
2X91
RA4
3X91
RA5
4X91
P/O A4/W2 TO
MICROPROCESSOR
BOARD A2
W2
J2(3)
9
BIT 40 FROM SHIFT REG
A4
8

SB 6 DEVICE BUS

CONTENTS

TABLES

FIGURE

INTRODUCTION

The device bus and control lines provide set-up data to the pulse generator circuits. See the block diagrams.

Device Bus

The control line and data interface in the controller translates the 8 line controller data bus into:

1. A 16 line data and address bus, the device bus
2. Three control lines, HINH, HDAT, and NDDV

Device Bus Latches and Decoders

The OUTPUT and TRIG OUTPUT functions contains latches and address decoders (acceptors) which generate the necessary pulses for latching the data required for a set-up.

Addressing and Data Transfer

The three control lines are:

1. HINH = HIGH INHIBIT
2. HDAT = HIGH DATA
3. NDDV = NOT DATA VALID.

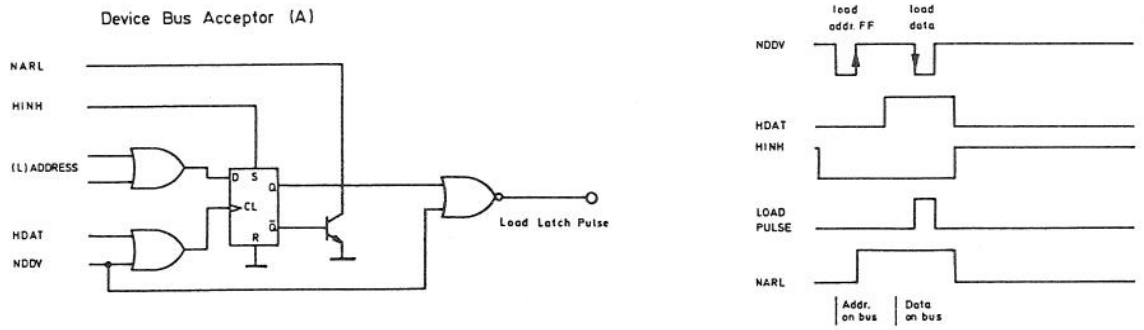
The transfer sequence (see Figure 1A/B, page 3.6-12 is as follows:

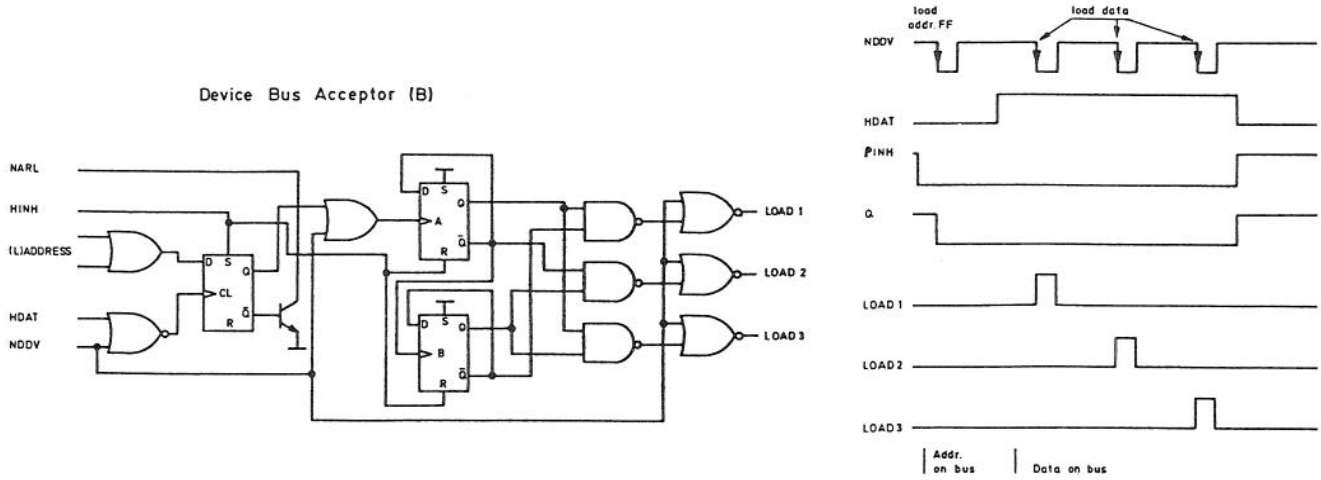
1. Start conditions.
   a. HINH = high
   b. HDAT = low
   c. NDDV = high.
2. Address sequence.
   a. HINH = low
   b. NDDV = low
   c. The address data is transmitted.
   d. NDDV = high
   e. Acceptor flip-flop output Q = low.
3. Data transfer sequence.
   a. HDAT = high
   b. Set-up data is transmitted.
   c. NDDV = low
   d. NDDV = high

Not Address Response Line, NARL

This signal line is a function of the action of the three control lines. It is returned to the controller's data bus to indicate whether the instrument has one channel or two channels.

FIGURE 1A AND 1B. Device Bus Acceptors.





TROUBLESHOOTING

The following tables contain the addresses and set-up data transmitted over the device bus to the pulse generator.

Data analysis requires the use of a logic analyzer.

1. Connect the analyzer to any device bus connector via an extender board.
2. Addressing and data transfer occur when a MODE or ENTRY button is pressed or a message unit is processed.
3. The transfer consists of 2-4 steps. The first step is always an address transfer.
4. The transfer steps are in Tables 10, 20, 30 40, 50, 60, 70, and 80.

   The set-up data are contained in Tables 11, 21, etc.

TABLE 10
FUNCTION ADDRESSES

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 1 1 1	1 1 0 1	1 1 1 1	0 1 1 1	BURST
1 1 1 1	1 1 1 1	0 1 1 1	1 1 1 0	PERIOD
1 1 1 1	1 0 1 1	1 1 1 1	1 1 1 0	DELAY A
1 1 1 1	0 1 1 1	1 1 1 1	1 1 1 0	DELAY B
1 1 1 1	1 0 1 1	1 1 1 1	1 1 0 1	WIDTH A
1 1 1 1	0 1 1 1	1 1 1 1	1 1 0 1	WIDTH B
1 1 1 0	1 1 1 1	1 1 1 1	1 1 1 0	SLOPE A
1 1 1 0	1 1 1 1	1 1 1 1	1 1 0 1	SLOPE B
1 1 0 1	1 1 1 1	1 1 1 1	1 1 1 0	OUTPUT A
1 1 0 1	1 1 1 1	1 1 1 1	1 1 0 1	OUTPUT B
1 1 1 1	1 1 1 0	1 1 1 1	1 0 1 1	INPUT MODE
1 0 1 1	1 1 1 1	1 1 1 1	1 1 1 0	OUTPUT MODE
1 0 1 1	1 1 1 1	1 1 1 1	1 1 0 1	REF TRIG WIDTH

TABLE 20
INPUT MODE
DATA TRANSFER

The Input Mode transfer is a two step transfer and is followed by the Reference Trigger transfer.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 1 1 1	1 1 1 0	1 1 1 1	1 0 1 1	INPUT MODE ADDRESS

2. DATA.

X X X X	X X X X	X X X X	X X X X	INPUT MODE DATA (TABLE 21)

TABLE 21
INPUT MODE
DATA

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	
0 - 1 1	1 1 0 0	0 0 0 0	0 0 0 0	NORM
0 - 0 1	1 0 0 0	- - - -	- - - -	GATE
0 - 1 0	1 0 1 0	- - - -	- - - -	EXT TRIG
0 - 1 1	0 1 0 0	- - - -	- - - -	BURST
0 1 0 0	0 0 0 0	- - - -	- - - -	POS SLOPE
0 0 0 0	0 0 0 0	- - - -	- - - -	NEG SLOPE
- - - -	- - - -	0 1 0 0	0 0 0 0	SINGLE PULSE
1 - - -	- - - -	- - - -	- - - -	MANUAL

TABLE 30
PERIOD DATA TRANSFER

The Period transfer is a two step transfer and is followed by the Reference Trigger transfer.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 1 1 1	1 1 1 1	0 1 1 1	1 1 1 0	PERIOD ADDRESS

2. DATA.

UNIT	DIGIT 6(MSD)	DIGIT 7	DIGIT 8(LSD)	PERIOD DATA
X X X X	X X X X	X X X X	X X X X	(TABLE 31)

TABLE 31
PULSE PERIOD DATA

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	
0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0	10.0 ns to
0 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1	99.9 ns
0 0 1 0	0 0 0 1	0 0 0 0	0 0 0 0	100 ns to
0 0 1 0	1 0 0 1	1 0 0 1	1 0 0 1	999 ns
0 0 1 1	0 0 0 1	0 0 0 0	0 0 0 0	1 us to
0 0 1 1	1 0 0 1	1 0 0 1	1 0 0 1	9.99 us
0 1 0 0	0 0 0 1	0 0 0 0	0 0 0 0	10.0 us to
0 1 0 0	1 0 0 1	1 0 0 1	1 0 0 1	99.9 us
0 1 0 1	0 0 0 1	0 0 0 0	0 0 0 0	100 us to
0 1 0 1	1 0 0 1	1 0 0 1	1 0 0 1	999 us
0 1 1 0	0 0 0 1	0 0 0 0	0 0 0 0	1 ms to
0 1 1 0	1 0 0 1	1 0 0 1	1 0 0 1	9.99 ms
0 1 1 1	0 0 0 1	0 0 0 0	0 0 0 0	10.0 ms to
0 1 1 1	1 0 0 1	1 0 0 1	1 0 0 1	99.9 ms
1 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	100 ms to
1 0 0 0	1 0 0 1	1 0 0 1	1 0 0 1	999 ms

TABLE 40
TIME INTERVAL
DATA TRANSFER

The Time Interval transfer is a 4 step transfer.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 1 1 1	1 0 1 1	1 1 1 1	1 1 1 0	DELAY A ADDRESS
1 1 1 1	0 1 1 1	1 1 1 1	1 1 1 0	WIDTH A ADDRESS
1 1 1 1	1 0 1 1	1 1 1 1	1 1 0 1	DELAY A ADDRESS
1 1 1 1	0 1 1 1	1 1 1 1	1 1 0 1	WIDTH B ADDRESS

2. The first data step transfers data for values < 50 ns.

T3	T2	T1		
X X X X	X X X X	X X X X	X X X X	0 to 49.9 ns (TABLES 41/42/43)

3. The second data step transfers data for values >= 50 ns to 450 ns.

N44 TO N41	N34 TO N31	N24 TO N21	N14 TO N11	
X X X X	X X X X	X X X X	X X X X	50 ns TO 450 us (TABLE 44)

4. The third data step transfers data for values >= 500 to 999 ms.

DBL	N81	N71 TO N71	N64 TO N61	N54 TO N51	
Y Y Y	X	X X X X	X X X X	X X X X	0.5 ms TO 999 ms (TABLE 44)

NOTE: Y Y Y = Double Pulse; see the following example.

EXAMPLE: This example shows the third and fourth steps when 99.9 ms and DOUBLE PULSE are selected.

1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	Step 3
0 1 0 0	0 0 0 1	1 0 0 1	1 0 0 1	Step 4

TABLE 41 T1 (0 ns to 0.9 ns)

	bit 8 (0.5 ns)	bit 7 (0.2 ns)	bit 6 (0.2 ns)	bit 5 (0.1 ns)
0 ns	0	0	0	0
0.1 ns	0	0	0	1
0.2 ns	0	0	1	0
0.3 ns	0	0	1	1
0.4 ns	0	1	1	0
0.5 ns	1	0	0	0
0.6 ns	1	0	0	1
0.7 ns	1	0	1	0
0.8 ns	1	0	1	1
0.9 ns	1	1	1	0

TABLE 42 T2 (1 ns to 9 ns)

	bit 12 (4 ns)	bit 11 (3 ns)	bit 10 (2 ns)	bit 9 (1 ns)
< 1 ns	0	0	0	0
1 ns	0	0	0	1
2 ns	0	0	1	0
3 ns	0	1	0	0
4 ns	1	0	0	0
5 ns	1	0	0	1
6 ns	1	0	1	0
7 ns	1	1	0	0
8 ns	1	1	0	1
9 ns	1	1	1	0

TABLE 43 T3 (10 ns to 40 ns)

	bit 15 (20 ns)	bit 14 (10 ns)	bit 13 (10 ns)
< 10 ns	0	0	0
10 ns	0	0	1
20 ns	0	1	1
30 ns	1	0	1
40 ns	1	1	1

TABLE 44
DATA LIST

N81		N71 to N74	N61 to N64	N51 to N54	N41 to N44	N31 to N34	N21 to N24	N11 to N14	T3	T2	T1
999 ms	1	9	9	8	0	0	0	0	0	0	0
99.9 ms	0	1	9	9	8	0	0	0	0	0	0
10.1 ms	0	0	2	0	2	0	0	0	0	0	0
10.0 ms	0	0	2	0	0	0	0	0	0	0	0
9.99 ms	0	0	1	9	9	8	0	0	0	0	0
1.01 ms	0	0	0	2	0	2	0	0	0	0	0
1.00 ms	0	0	0	2	0	0	0	0	0	0	0
999 us	0	0	0	1	9	9	8	0	0	0	0
10.1 us	0	0	0	0	0	2	0	2	0	0	0
10.0 us	0	0	0	0	0	2	0	0	0	0	0
9.99 us	0	0	0	0	0	1	9	9	4	0	0
9.98 us	0	0	0	0	0	1	9	9	3	0	0
1.00 us	0	0	0	0	0	0	2	0	0	0	0
999 ns	0	0	0	0	0	0	1	9	4	9	0
998 ns	0	0	0	0	0	0	1	9	4	8	0
100 ns	0	0	0	0	0	0	0	2	0	0	0
99.0 ns	0	0	0	0	0	0	0	1	4	9	9
01.0 ns	0	0	0	0	0	0	0	0	0	1	0
00.9 ns	0	0	0	0	0	0	0	0	0	0	9
000 ns	0	0	0	0	0	0	0	0	0	0	0

TABLE 50
SLOPE DATA
TRANSFER

The Slope transfer is a three step transfer.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 1 1 0	1 1 1 1	1 1 1 1	1 1 1 0	SLOPE A ADDRESS
1 1 1 0	1 1 1 1	1 1 1 1	1 1 0 1	SLOPE B ADDRESS

2. DATA (LEE).

UNIT	DIGIT 6(MSD)	DIGIT 7	DIGIT 8(LSD)	
X X X X	X X X X	X X X X	X X X X	LEE DATA (TABLE 51)

3. DATA (TRE).

	DIGIT 6(MSD)	DIGIT 7	DIGIT 8 (LSD)	
X X X X	X X X X	X X X X	X X X X	TRE DATA (TABLE 51)

TABLE 51
SLOPE DATA

NOTE: The 'UNIT' data is transferred in step 2, LEE data transfer.

UNIT 16 15 14 13	DIGIT 6(MSD) 12 11 10 9	DIGIT 7 8 7 6 5	DIGIT 8(MSD) 4 3 2 1	SLOPE GENERATOR RANGES
				RANGE 1
0 0 0 1	0 0 0 0	0 1 1 0	0 0 0 0	6.0 ns to
0 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1	99.9 ns
				RANGE 2
0 0 1 0	0 0 0 0	0 1 0 1	0 0 0 0	50 ns to
0 0 1 0	1 0 0 1	1 0 0 1	1 0 0 1	999 ns
				RANGE 3
0 0 1 1	0 0 0 0	0 1 0 1	0 0 0 0	0.50 us to
0 0 1 1	1 0 0 1	1 0 0 1	1 0 0 1	9.99 us
				RANGE 4
0 1 0 0	0 0 0 0	0 1 0 1	0 0 0 0	5.0 us to
0 1 0 0	1 0 0 1	1 0 0 1	1 0 0 1	99.9 us
				RANGE 5
0 1 0 1	0 0 0 0	0 1 0 1	0 0 0 0	50 us to
0 1 0 1	1 0 0 1	1 0 0 1	1 0 0 1	999 us
				RANGE 6
0 1 1 0	0 0 0 0	0 1 0 1	0 0 0 0	0.5 ms
0 1 1 0	1 0 0 1	1 0 0 1	1 0 0 1	9.99 ms

TABLE 60
OUTPUT LEVEL
DATA TRANSFER

The OUTPUT Level is a three step transfer and is followed by the OUTPUT MODE transfer.

If the amplitude is => 2.0 V, the amplitude is transferred twice. The first transfer sequence sets the amplifier to x1, and the second sequence transfers the actual data.

NOTES:
1. OUTPUT DISABLE causes different data.
2. Amplitude = HIL - LOL.
3. Step size below 10 V from 50 ohm into 50 ohm is 10 mV.
4. Step size below 10 V from 1 k ohm into 50 is 20 mV.
5. Step size below 10 V from 1 k ohm into 50 ohm is 100 mV.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 1 0 1	1 1 1 1	1 1 1 1	1 1 1 0	OUTPUT A ADDRESS
1 1 0 1	1 1 1 1	1 1 1 1	1 1 0 1	OUTPUT B ADDRESS

2. DATA.

				FUNCTION
X X X X	X X X X	X X X X	X X X X	OUTPUT DATA (TABLES 61 TO 67)

NOTE: Bits 5-9 = offset data
Bits 1-4 = gain

3. DATA TRANSFER

				FUNCTION
X X X X	X X X X	X X X X	X X X X	OUTPUT DATA (TABLES 61 TO 67)

NOTE: Bits 9-16 = amplitude data.
Bits 1-8 = offset data

TABLE 61
AMPLITUDE AND GAIN DATA 1V-1.99V

The digital step size between 1 V (100 mV) and 1.99 V (1999 mV) is 2.

1. The LSB (9) is not used.
2. 99 steps allowed.
3. The output gain = x1.

NOTE: LOL = 0 V.

	STEP 3 AMPLITUDE								STEP 2 GAIN				
	16	15	14	13	12	11	10	9	4	3	2	1	VERNIER OUTPUT
HIL 1 V (100 mV)	1	1	0	0	1	0	0	0	1	0	1	1	1.0 V swing (100 mV)
HIL 1.1 V (110 mV)	1	0	1	1	0	1	0	0	1	0	1	1	1.1 V swing (110 mV)
HIL 1.34 V	1	0	0	0	0	1	0	0	1	0	1	1	1.34 V swing
HIL 1.35 V	1	0	0	0	0	0	1	0	1	0	1	1	1.35 V swing
HIL 1.98 V	0	0	0	0	0	1	0	0	1	0	1	1	1.98 V swing
HIL 1.99 V	0	0	0	0	0	0	1	0	1	0	1	1	1.99 V swing

TABLE 62
AMPLITUDE AND GAIN DATA
2V-9.99V

The digital step size between 2 V (200 mV) and 3.99 V (399 mV) is 1.

1. The LSB (9) is used.
2. 199 steps.
3. Output gain = x2.
4. Valid for all amplitudes => 2.0 V.

NOTE: LOL = 0 V.

	STEP 3 AMPLITUDE								STEP 2 GAIN				
	16	15	14	13	12	11	10	9	4	3	2	1	VERNIER OUTPUT
HIL 2.0 V (200 mV)	1	1	0	0	1	0	0	0	0	0	1	1	1 V swing (100 mV)
HIL 2.2 V (220 mV)	1	0	1	1	0	1	0	0	0	0	1	1	1.1 V swing (110 mV)
HIL 3.98 V	0	0	0	0	0	0	1	0	0	0	1	1	1.98 V swing
HIL 3.99 V	0	0	0	0	0	0	0	1	0	0	1	1	1.99 V swing
HIL 4.00 V (400 mV)	1	1	0	0	1	0	0	0	0	0	1	0	2.00 V swing
HIL 5.99 V	0	0	0	0	0	0	0	1	0	0	1	0	2.99 V swing
HIL 6.00 V (600 mV)	1	1	0	0	1	0	0	0	0	0	0	1	3.00 V swing
HIL 8.00 V (800 mV)	1	1	0	0	1	0	0	0	0	0	0	0	4.00 V swing (400 mV)
HIL 9.99 V	0	0	0	0	0	1	0	1	0	0	0	0	4.99 V swing (500 mV)

TABLE 63
AMPLITUDE AND GAIN DATA 10V-19.9V

The digital step size between 10 V and 19.9 V is 5. Thus, the amplitude changes by 100 mV per step.

NOTE: LOL = 0 V.

	STEP 3 AMPLITUDE								STEP 2 GAIN				
	16	15	14	13	12	11	10	9	4	3	2	1	VERNIER OUTPUT
HIL 10.0 V	0	1	1	0	0	1	0	0	0	0	1	0	2.5 V swing
HIL 15.0 V	0	0	1	1	0	0	1	0	0	0	0	1	3.75 V swing
HIL 19.8 V	0	0	0	0	1	0	1	0	0	0	0	0	4.95 V swing
HIL 19.9 V	0	0	0	0	0	1	0	1	0	0	0	0	4.98 V swing

TABLE 64
OFFSET DATA
<1V (50 OHM)

Offset = HIL+LOL/2 (maximum 10 V into 50 ohm).

The smallest step is 5 between 0v and 995 mV offset generater output (The offset generator is set to x 0.1).

STEP 3 OFFSET								STEP 2 OFFSET				
8	7	6	5	4	3	2	1	8	7	decimal	HIL	LOL
0	0	0	0	0	0	0	0	0	0	0	0.1 V	-0.1 V
0	0	0	0	0	0	0	1	0	1	5	0.11 V	-0.1 V
0	0	0	0	0	0	1	0	1	0	10	0.12 V	-0.1 V
1	1	1	1	0	1	1	1	1	0	990	1.98 V	0 V
1	1	1	1	1	0	0	0	1	1	995	1.99 V	0 V

TABLE 65
OFFSET DATA
1V-10V (50 OHM)

The digital step size per 100 mV amplitude change is 5 between 1.00 V and 10.0 V offset generator output (The offset generator is set to x1).

STEP 3 OFFSET								STEP 2 OFFSET				
8	7	6	5	4	3	2	1	8	7	decimal	HIL	LOL
0	1	1	1	1	0	1	0	1	0	490	9.80 V	0 V
0	1	1	1	1	0	0	1	0	1	485	9.70 V	0 V
0	0	1	1	1	1	1	0	1	0	250	5.00 V	0 V
0	0	0	1	1	0	1	1	1	0	110	2.20 V	0 V
0	0	0	1	1	0	1	0	0	1	105	2.10 V	0 V

TABLE 66
OFFSET DATA
10-19.9V (1K OHM)

The smallest digital step is 2 (even) or 3 (odd) in the amplitude range 10 V to 19.9 V (1 k ohm)

STEP 3 OFFSET								STEP 2 OFFSET				
8	7	6	5	4	3	2	1	8	7	decimal	HIL	LOL
0	0	1	1	1	1	1	0	1	0	230	10.0 V	0 V
0	1	0	1	0	1	0	1	1	1	343	15.0 V	0 V
0	1	1	1	1	1	0	0	0	1	497	19.9 V	0 V
0	1	0	0	1	0	0	0	0	0	288	10.5 V	10.0 V
1	1	1	1	0	1	1	1	1	0	990	19.9 V	19.7 V

TABLE 67
OFFSET GAIN AND POLARITY

	bit 9	bit 6	bit 5
POSITIVE	0	0	-
NEGATIVE	1	1	-
ZERO	0	1	-
x0.1	-	-	1
x1	-	-	0

TABLE 70
SHIFT SUPPLY AND OUTPUT MODE DATA TRANSFER

The Shift Supply and OUTPUT Mode transfer is a 2 step transfer.

If 50 ohm or 1 k ohm is selected, the Amplitude transfer follows.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 0 1 1	1 1 1 1	1 1 1 1	1 1 1 0	OUTPUT MODE ADDRESS

2. DATA.

SHIFT SUPPLY DATA (9-16)				OUTPUT MODE DATA (1-8)				
X X X X	X X X X			X X X X	X X X X			OUTPUT MODE DATA (TABLES 71, 72)

TABLE 71
SHIFT SUPPLY DATA

16 15 14 13	12 11 10 9	decimal	SHIFT OUTPUT
0 0 0 0	0 0 0 1	1	-10.0 V
0 1 1 0	0 1 0 0	100	0 V
1 1 0 0	0 1 1 0	198	+10.0 V

TABLE 72
OUTPUT MODE DATA

	bit value = 0	bit value = 1
bit 1	A SEP B	A ADD B
bit 2	NORM (A)	COMP (A)
bit 3	50 OHM (A)	1 k OHM (A)
bit 4	Disable (A)	Enable (A)
bit 5	NORM (B)	COMP (B)
bit 6	50 Ohm (B)	1 k Ohm (B)
bit 7	Disable (B)	Enable (B)
bit 8	-	-

TABLE 80
REFERENCE TRIGGER
DATA TRANSFER

The Reference Trigger transfer is a two step transfer.
An INPUT MODE transfer or a PERIOD transfer occurs first.

1. ADDRESS.

16 15 14 13	12 11 10 9	8 7 6 5	4 3 2 1	FUNCTION
1 0 1 1	1 1 1 1	1 1 1 1	1 1 0 1	REFERENCE TRIGGER ADDRESS

2. DATA.

-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	REFERENCE TRIGGER DATA (TABLE 81)

TABLE 81
REFERENCE TRIGGER DATA

The 10-50MHz range applies to the NORM, GATE, TRIG, and BURST INPUT modes.

The 1-9.9MHz and 0.9Hz-0.99MHz ranges apply to the NORM, GATE, and BURST INPUT modes.

	8 ns	40 ns	400 ns
bit 1	0	1	0
bit 2	0	0	1
Rate Generator (VCO frequency)	10-50 MHz	1-9.9MHz	0.9Hz-0.99MHz

SB 7 REPETITION RATE GENERATOR

CONTENTS

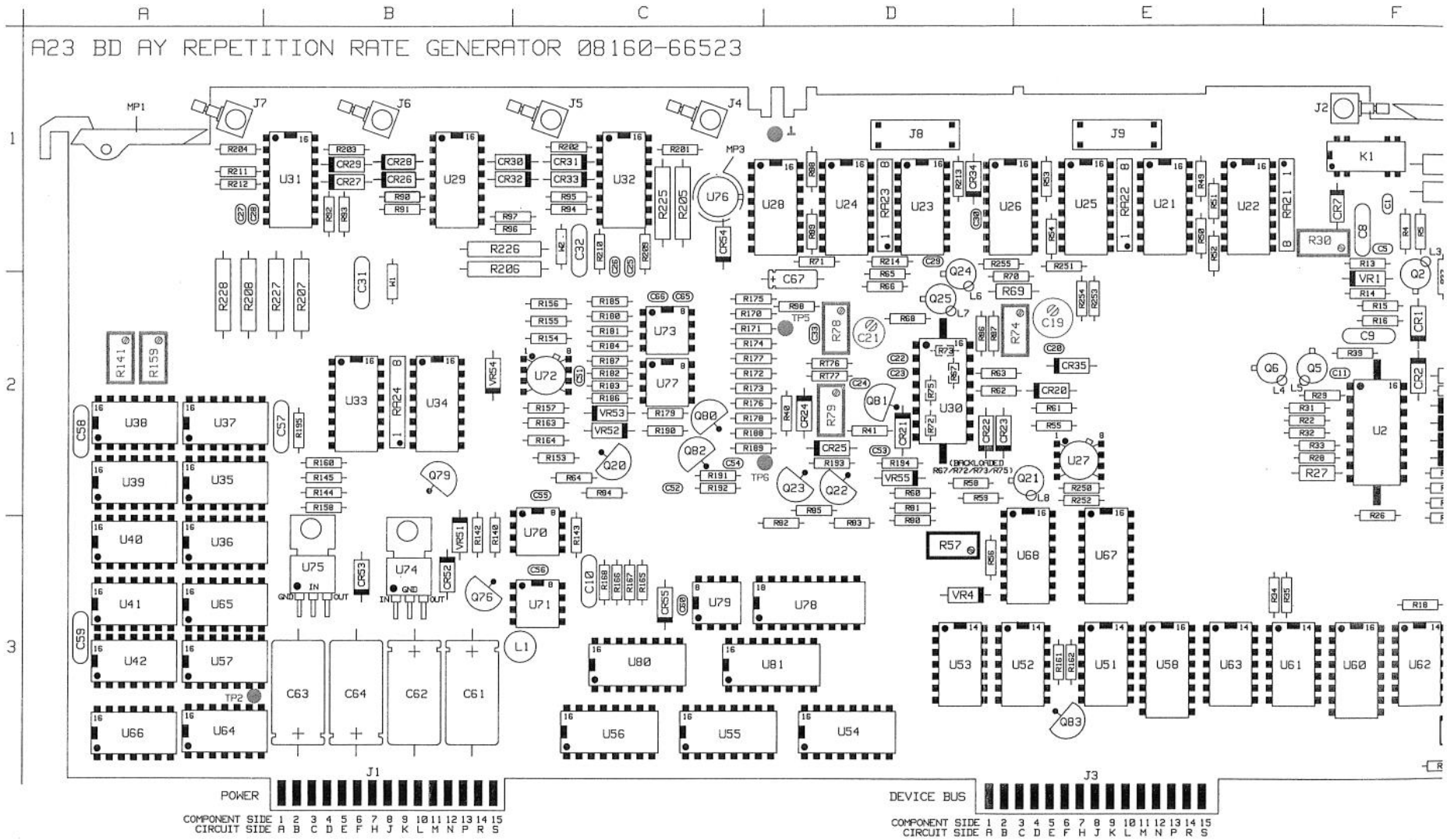
ASSEMBLIES

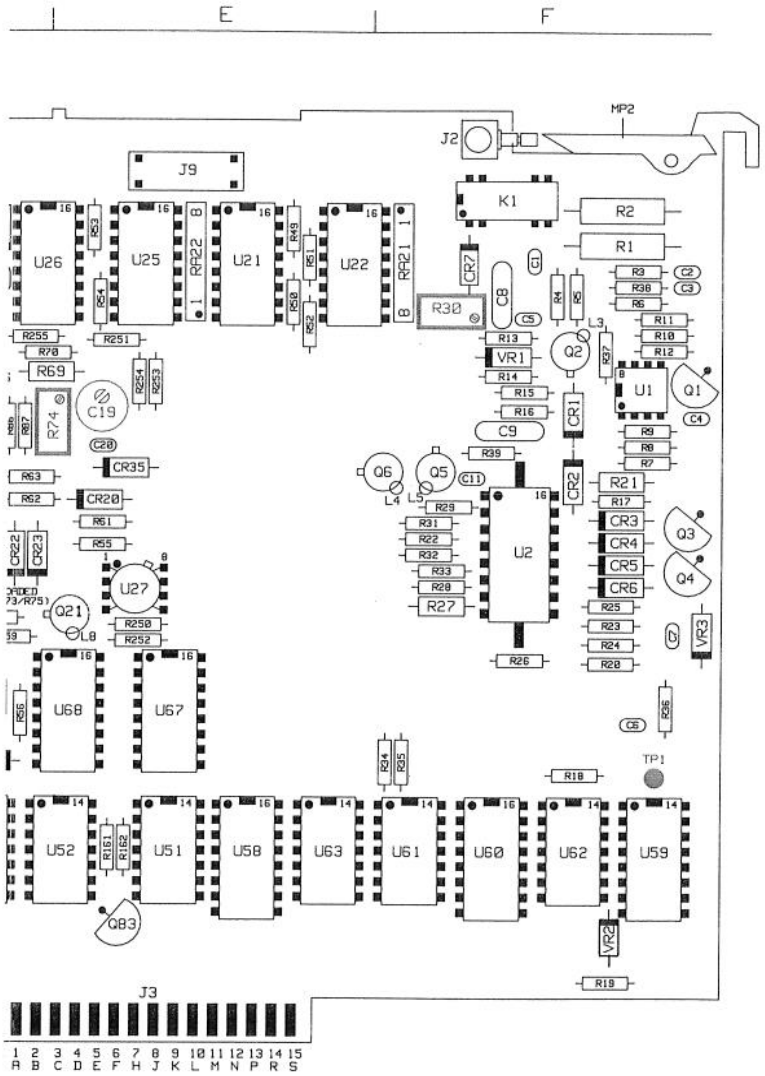
COMPONENT LAYOUT DIAGRAM

SCHEMATIC DIAGRAMS

FIGURE

TABLES


A23 BD AY REPETITION RATE GENERATOR 08160-66523
A
B
C
D
E
F
1
2
3
MP1
J7
J6
J5
J4
J8
J9
J2
K1
MP3
U31
U29
U32
U76
U28
U24
U23
U26
U25
U21
U22
R30
U73
U72
U77
U33
U34
U38
U37
U39
U35
U40
U36
U41
U65
U42
U57
U66
U64
U75
U74
U70
U71
U79
U78
U80
U81
U56
U55
U54
U68
U67
U53
U52
U51
U58
U63
U61
U60
U62
U30
U27
U2
Q20
Q79
Q80
Q82
Q81
Q23
Q22
Q21
Q83
Q76
Q24
Q25
Q6
Q5
Q2
C67
C63
C64
C62
C61
L1
TP2
TP5
TP6
J1
POWER
COMPONENT SIDE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
CIRCUIT SIDE A B C D E F H J K L M N P R S
J3
DEVICE BUS
COMPONENT SIDE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
CIRCUIT SIDE A B C D E F H J K L M N P R S



REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
C1	F1	CR26	B1	R4	F1	R67	D2	R174	C2	TP1	F3	U79	C3
C2	F2	CR27	B1	R5	F1	R68	D2	R175	C2	TP2	A3	U80	C3
C3	F2	CR28	B1	R6	F1	R69	E2	R176	C2	TP5	D2	U81	D3
C4	F2	CR29	B1	R7	F2	R70	E2	R177	C2	TP6	D2		
C5	F2	CR30	C1	R8	F2	R71	D2	R178	C2			VR1	F2
										U1	F2	VR2	F3
C6	F3	CR31	C1	R9	F2	R72	D2	R179	C2	U2	F2	VR3	D3
C7	F3	CR32	C1	R10	F2	R73	D2	R180	C2	U21	E1	VR4	E3
C8	F1	CR33	C1	R11	F2	R74	E2	R181	C2	U22	E1	VR51	B3
C9	F2	CR34	D1	R12	F2	R75	D2	R182	C2	U23	D1		
C10	C3	CR35	E2	R13	F2	R78	D2	R183	C2			VR52	C2
										U24	D1	VR53	C2
C11	F3	CR52	B3	R14	F2	R79	D2	R184	C2	U25	E1	VR54	B2
C19	E2	CR53	B3	R15	F2	R80	D3	R185	C2	U26	D/E1	VR55	D2
C20	E2	CR54	C1	R16	F2	R81	D3	R186	C2	U28	D1		
C21	D2	CR55	C3	R17	F2	R82	D3	R187	C2	U29	B1	W1	B2
C22*	D2			R18	F3	R83	D3	R188	C2			W2	C2
		J2	F1							U30	D2		
C23	D2	J4	C1	R19	F3	R84	C3	R189	C2	U31	B1		
C24	D2	J5	C1	R20	F3	R85	D3	R190	C2	U32	C1		
C25	C2	J6	B1	R21	F2	R86	D2	R191	C2	U33	B2		
C26	C2	J7	A1	R22	F2	R87	D2	R192	C2	U34	B2		
C27	A1	J8	D1	R23	F3	R88	D1	R193	D2				
		J9	E1							U35	A2		
C28	A1			R24	F3	R89	D2	R194	D2	U36	A3		
C29	D2			R25	F2	R90	B1	R195	B2	U37	A2		
C30	D1	K1	F1	R27	F3	R91	B1	R201	C1	U38	A2		
C31	B2			R28	F2	R92	B1	R202	C1	U39	A2		
C32	C1	L1	B3	R29	F2	R93	B1	R203	B1				
		L3	F1							U40	A3		
C33	D2	L4	F2	R30	F1	R94	C1	R204	B1	U41	A3		
C51	C2	L5	F2	R31	F2	R95	C1	R205	C1	U42	A3		
C52	C2	L6	D2	R32	F2	R96	B1	R206	B2	U51	E3		
C53	D2	L7	D2	R33	F2	R97	B1	R207	B2	U52	E3		
C54	C2	L8	E2	R34	F3	R98	D2	R208	A2				
										U53	D3		
C55	C2	MP1	A1	R35	F3	R140	B3	R209	C2	U54	D3		
C56	C3	MP2	A1	R36	F2	R141	A2	R210	C2	U55	C3		
C57	B2	MP3	C1	R37	F1	R142	B3	R211	A1	U56	C3		
C58	A2			R38	F1	R143	C3	R212	A1	U57	A3		
C59	A3	Q1	F2	R39	F2	R144	B2	R213	D1				
		Q2	F2							U58	E3		
C60	C3	Q3	F2	R40	D2	R145	B2	R214	D2	U59	F3		
C61	B3	Q4	F2	R41	D2	R153	C2	R225	C1	U60	F3		
C62	B3	Q5	F2	R49	E1	R154	C2	R226	B2	U61	F3		
C64	B3			R50	E1	R155	C2	R227	B2	U62	F3		
C65	C2	Q6	F2	R51	E1	R156	C2	R228	A2				
C66	C2	Q20	C2							U63	E3		
C67	D2	Q21	E2	R52	E1	R157	C2	R250	E3	U64	A3		
		Q22	D2	R53	E1	R159	A2	R251	E2	U65	A3		
CR1	F2	Q23	D2	R54	E1	R160	B2	R252	E3	U66	A3		
CR2	F2			R55	E2	R161	E3	R253	E2	U67	E3		
CR3	F2	Q24	D2	R56	D3	R162	E3	R254	E2				
CR4	F2	Q25	D2					R255	D2	U68	E3		
CR5	F2	Q76	B3	R57	D3	R163	C2			U70	C3		
		Q79	B2	R58	D2	R164	C2			U71	C3		
CR6	F2	Q80	C2	R59	D3	R165	C3	RA221	F1	U72	C2		
CR7	F1			R60	D3	R166	C3	RA222	E1	U73	C2		
CR20	E2	Q81	D2	R61	E2	R167	C3	RA223	D1				
CR21	D2	Q82	C2					RA224	B2	U74	B3		
CR22	D2	Q83	E3	R62	D2	R168	C3			U75	B3		
				R63	D2	R170	C2	RT76	D2	U76	C1		
CR23	D2	R1	F1	R64	C2	R171	C2	RT77	D2	U77	C2		
CR24	D2	R2	F1	R65	D2	R172	C2			U78	D3		
CR25	D2	R3	F1	R66	D2	R173	C2						

INTRODUCTION

The repetition rate generator provides the following signals:

1. OUTPUT 1 = Channel 1 = OUTPUT A
2. OUTPUT 2 = Channel 2 = OUTPUT B
3. OUTPUT 3 = Not used.
2. OUTPUT 4 = Reference Trigger = TRIG OUTPUT.

The pulse is an EECL signal with a width of 3 ns.

The repetition rate generator free runs in the normal operating mode and is controlled in the triggered, gated, and burst operating modes.

The burst mode operation is describe in SB 8, BURST.

The controlled operating modes can be stimulated by an External Input signal or the Manual stimulus.

The EXT INPUT trigger level, impedance, slope, and signal conditioning circuits are on the Repetition Rate Generator assembly.

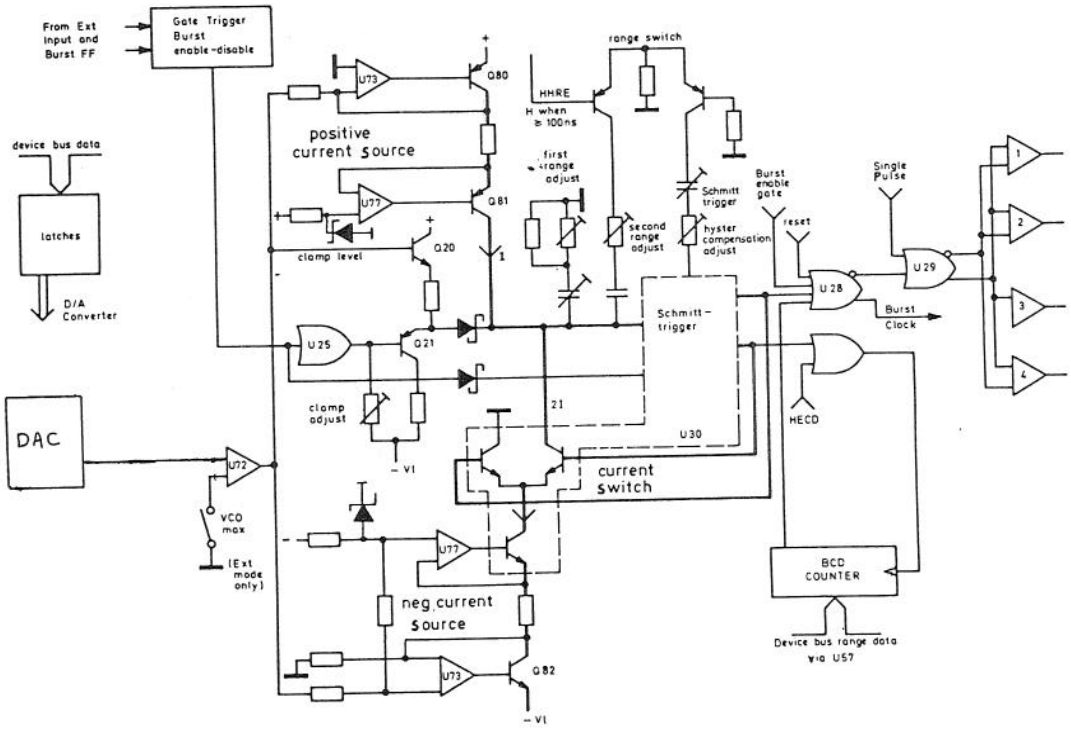
The Manual stimulus mode operates through the EXT INPUT slope circuits. Thus, it acts like a controlled operating mode.

The Single Pulse stimulus mode is accomplished by gating the output of the VCO.

The Repetition Rate Generator consists of the following circuits:

1. Voltage Controlled Oscillator (VCO)
2. VCO control voltage
3. Exponent Counter
4. Operating Modes
    a. VCO Control Input
    b. Normal
    c. Gate
    d. Trigger
    e. Burst
5. Stimulus Modes
    a. EXT INPUT
    b. Manual
    c. Single Pulse
6. Output Buffer

FIGURE 1. Repetition Rate Generator.



VOLTAGE CONTROLLED OSCILLATOR CIRCUIT

Voltage Controlled Oscillator (VCO)

The control voltage for the VCO is generated by DAC A23/U78.

The VCO is the main circuit of the repetition rate generator. It consists of two basic circuits.

1. Ramp Generator
2. Schmitt Trigger.

The ramp generator consists of:

1. Ramp caps A23/C21-23
2. Positive Current Source A23/Q80 and Q81
3. Negative Current Source A23/Q82
4. Negative Current Switch A23/U30.

The ramp capacitors circuits are arranged to provide two ranges.

1. C21 and C22 are used for PER < 100 ns
2. C23 is switched into the circuit with C21 and C22 for Per >= 100 ns.

The ramp voltage developed at the capacitors serves as a trigger for the Schmitt Trigger.

The current sources provide current directly related to the VCO control voltage.

The negative current source is switched on and off by the negative current source switch.

Free-run Mode

When the current switch is off, the ramp voltage is positive. When the upper trigger point of the Schmitt Trigger is reached the outputs change and turn the current switch on.

Now, the ramp voltage is negative. When the lower trigger point is reached the outputs change and turn the current switch off.

The VCO outputs a pulse with a 50% duty cycle.

One VCO output goes to the Exponent Counter at A23/U37, and the other goes to gate A23/U28.

Clamp Circuit

When the VCO is switched off, the level at the ramp node remains stable at the lower trigger point because of the clamp circuit. In the VCO off state, the current switch is on and draws 2I. Thus, the clamp circuit must supply I. If I changes (PERIOD CHANGE), the clamp level is be adjusted to compensate the changing voltage drop at the Schottky diode A23/CR21. Thus, a constant level at the ramp node is maintained.

When the VCO is switched on, the clamping level is pulled down causing the Schottky diode to cutoff. This insures that the waveform at the ramp node is not distorted by an additional clamp current.

VCO Control Voltage

DAC data from the MPU is latched into A23/U54-56. The output of the latches provide the digital data to DAC A23/U78.

The DAC then outputs a control voltage to the positive and negative current source circuits and A23/Q20.

Exponent Counter

For PER <= 999 ns the exponent counter is disabled. And a VCO signal with the appropriate PERIOD is gated by A23/U28 to the output amplifier directly.

For PER > 999 ns the exponent counter is enabled and divides the VCO output by 10 to the n (n = 1-6) to create a signal with the correct period.

Counter data is latched from the device bus by A23/U57 and decoded by A23/U64.

Exponent counter control flip-flop A23/U23 enables gate A23/U28 which gates a VCO signal with the required period to the output buffer amplifier.

Exponent Counter Example

The exponent counter is set to devide by 10.

Exponent counter flip-flop A23/U23 is reset.
This loads the exponent counter as follows:
A23/U37 = 0(decimal)
A23/U38-U42 = 9(decimal).

Thus, U23/Pin 3 is high, and U28/Pin 12 is low which enables U28.

The next inverted VCO output pulse is gated through U28. The inverted output of U28/Pin 14 then sets control flip-flop U23.

Now, U28/Pin 12 is high and U28 is disabled.

The non-inverted VCO output is counted by the exponent counter and at the 9th pulse the count is 999999. This causes the input to U23/Pin 7 to go low.

This negative transistion of the non-inverted VCO signal inverted by A23/U24 clocks the low data into the control flip-flop.

Now, U23/Pin 3 is high which enables U28 and one inverted VCO pulse is gated by U28 to the output amplifier.

The inverted output of U28 sets the control flip-flop and U28 is disabled, and the count cycle is repeated.

OPERATING MODES

There are 4 operating modes:

1. NORMAL = The VCO free-runs.
2. GATE = The VCO is controlled.
3. TRIGGER = The VCO is controlled.
4. BURST= The VCO is controlled.

VCO Control Input

A23/U30 pin 10 is the control input of the VCO. A low level at this input (-2.0 V) enables the VCO and a high level (-1.1 V) disables the VCO.

The control signal is generated by A23/U21-23.

Normal Mode

In the normal operating mode, pin 10 is low and the VCO freeruns.

Gate Mode

In the gated operating mode, pin 10 is low for the duration fot the gate signal. The gating signal is gated by U21/pin 15.

Trigger Mode

In the triggered operating mode, pin 10 is low for 3 ns. This allows the VCO to generate one pulse.

The 3 ns pulse is generated by NORing the outputs of A23/U2 at A23/U22.

Burst Mode

In the burst operating mode, pin 10 is held low until the required number of pulses is generated by the VCO. A description of the burst mode and circuits is in Service Block 9.

STIMULUS MODES

There are 3 stimulus modes which control the VCO.

External Input

The external input circuits include the front panel input BNC connector, input switch, and the trigger level adjustment potentiometer.

These circuits select the input impedance, set the trigger level, and set the input slope polarity.

Manual

With the manual stimulus mode, the control of the VCO is as described for the trigger, gate, and burst operating modes.

However, the signal generated at U2/pin 8 results from the MANUAL pulse applied to the input slope circuit rather than an external input signal.

The MANUAL circuit action can be simulated with the external slope controls.

Single Pulse

With the single pulse stimulus mode, the VCO is freerunning. One VCO pulse is gated through A23/U28 by the single pulse control signal at U28/pin 7.

OUTPUT BUFFER AMPLIFIER

The two signals from U28/pin 3 and pin 2 are transmitted over striplines. One signal is delayed by 3 ns.

The signals are then gated by U29 resulting into four signals with 3 ns pulse widths.

The signals are then level shifted by A23/CR26-33 and buffered by A23/U31 and U32.

TROUBLESHOOTING The following six tables provide repetition rate generator data.

TABLE 1. TRIG LEVEL Voltages

POTENTIOMETER POSITION	U1/1	U1/7	Q2(base)	Q2(emitter)	U2/15
Clockwise (+10 V position)	12.4 V	-12.6 V	-5.9 V	-6.6 V	-2.5 V
3 position*	7.6 V	-7.7 V	-3.6 V	-4.3 V	-2.5 V
12 position*	1.5 V	-1.5 V	-0.7 V	-1.5 V	-1.3 V
9 position*	-5.4 V	5.4 V	2.4 V	1.7 V	0.0 V
Counter-Clockwise (+10 V position)	-9.1 V	9.2 V	4.1 V	3.4 V	0.0 V

* 'position' indicates the 9, 12, and 3 positions on a clock face.

TABLE 2. DAC Truth Table

NOTE: The DAC data is latched by:

1. A23/U56 = digit 6 = most significant digit of VALUE display
2. A23/U55 = digit 7
3. A23/U54 = digit 8 = least significant digit of VALUE display.

The logic levels in the following table are valid for each latch when a period value is displayed in the VALUE display.

DECIMAL NUMBER DISPLAYED	LATCH, PIN 10	LATCH, PIN 2	LATCH, PIN 11	LATCH, PIN 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	9	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

TABLE 3. PERIOD RANGES

RANGE	PERIOD	U57 PIN 1	U57 PIN 11	U57 PIN 10	U57 PIN 2
1	20 ns - 99.9 ns	0	0	0	1
2	100 ns - 999 ns	0	0	1	0
3	1 us - 9.99 us	0	0	1	1
4	10.0 us - 99.9 us	0	1	0	0
5	100 us - 999 us	0	1	0	1
6	1 ms - 9.99 ms	0	1	1	0
7	10 ms - 99.9 ms	0	1	1	1
8	100 ms - 999 ms	1	0	0	0

TABLE 4. Voltage Controlled Current Sources

NOTE: 'ms' and 'us' magnitudes use the same period value-pattern described in the following table for 'ns'.

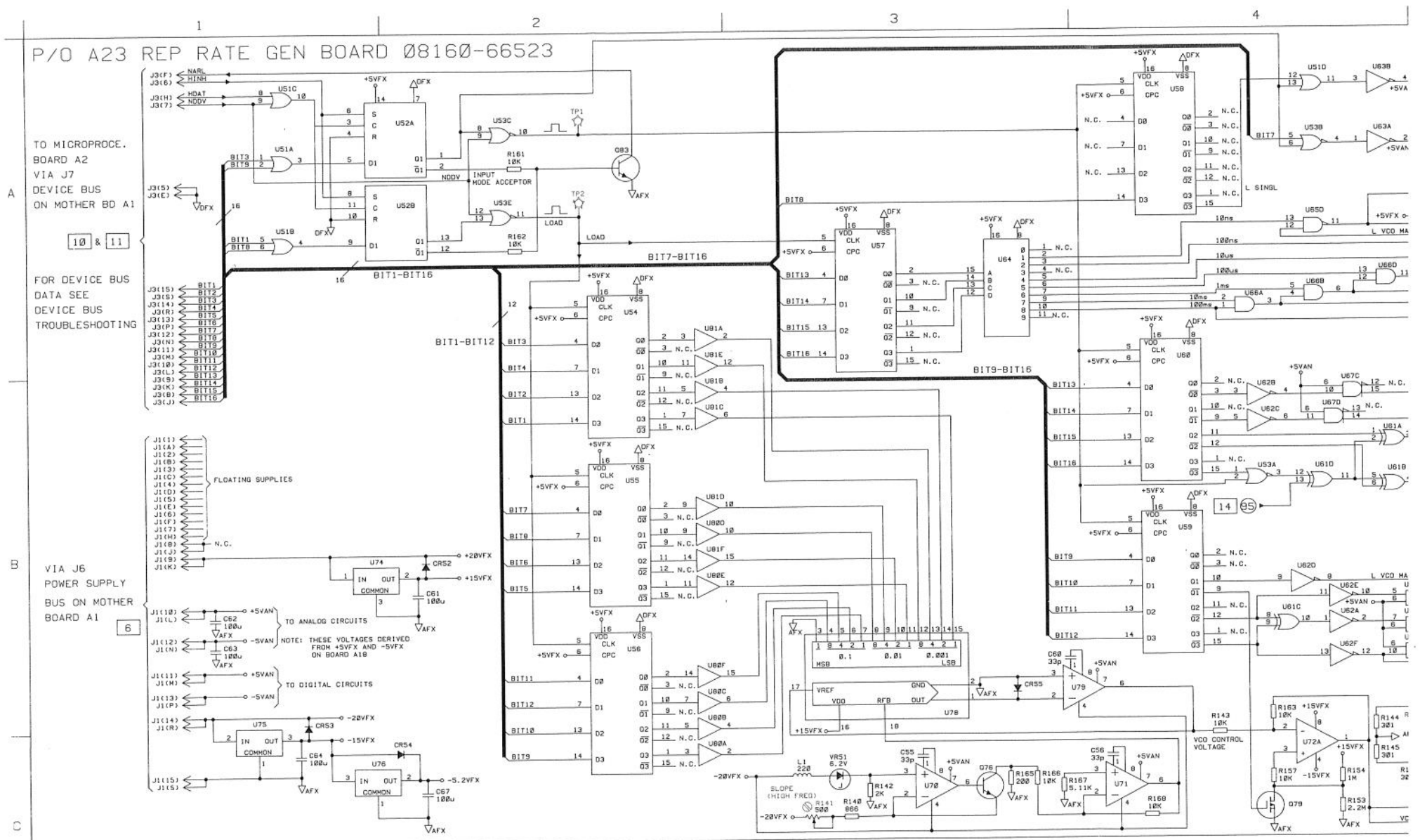
PERIOD	A23/U79 PIN 6	A23/U72 PIN 1	TP 5	A23/U73 PIN 7	A23/U73 PIN 1
18.0 ns	-5.9 V	5.9 V	-2.9 V	8.0 V	-7.6 V
25.0 ns	-4.2 V	4.2 V	-2.1 V	9.0 V	-8.5 V
50.0 ns	-2.1 V	2.1 V	-1.1 V	10.0 V	-9.7 V
75.0 ns	-1.4 V	1.4 V	-0.7 V	10.4 V	-9.0 V
99.9 ns	-1.1 V	1.1 V	-0.5 V	10.6 V	-10.3 V
100.0 ns	-10.8 V	10.8 V	-5.4 V	5.3 V	-5.1 V
500 ns	-2.1 V	2.1 V	-1.1 V	10.0 V	-9.7 V
999 ns	-1.1 V	1.1 V	-0.5 V	10.6 V	-10.3 V
1.0 us	-10.8 V	10.8 V	-5.6 V	5.2 V	-5.12 V
TRIG MODE			-6.6 V	+3.9 V	-3.5 V

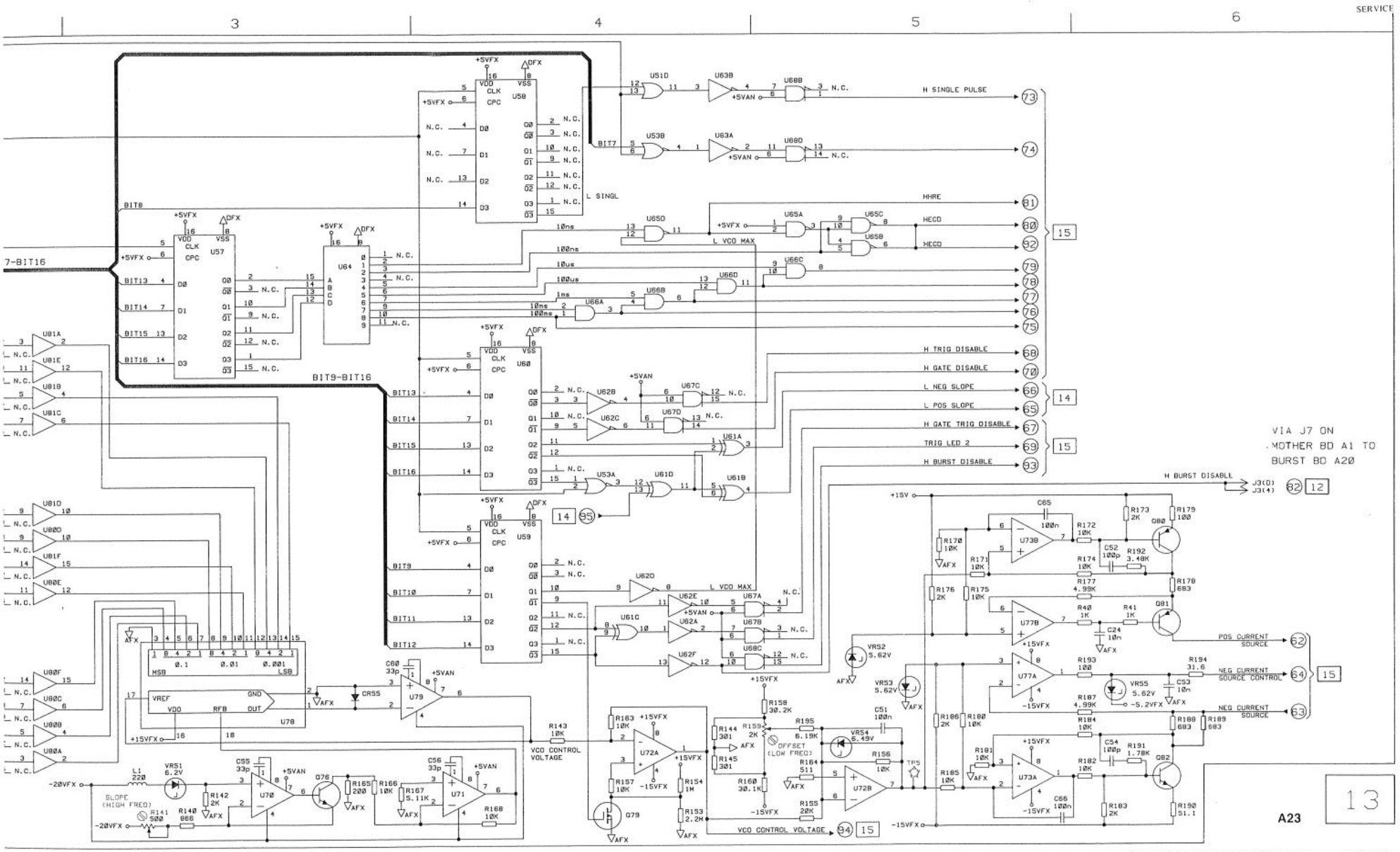
TABLE 5. INPUT MODE TRUTH TABLE

SIGNAL	NORM	TRIG	GATE	BURST	POS	NEG
H POS SLOPE "65"	-	-	-	-	0	1
H NEG SLOPE "66"	-	-	-	-	1	0
H GATE DIS "67"	1	0	0	1	-	-
H TRIG DIS "68"	1	0	1	1	-	-
TRIG LED 2 "69"	1	0	0	0	-	-
H G DIS "70"	1	1	0	1	-	-
H SINGLE PULSE "73"	-	SINGLE PULSE PRODUCES A POSITIVE PULSE				-
"74	-	POSITIVE PULSE WHEN THE INPUT MODE IS CHANGED				
H BURST DIS "93"	1	1	1	0	-	-

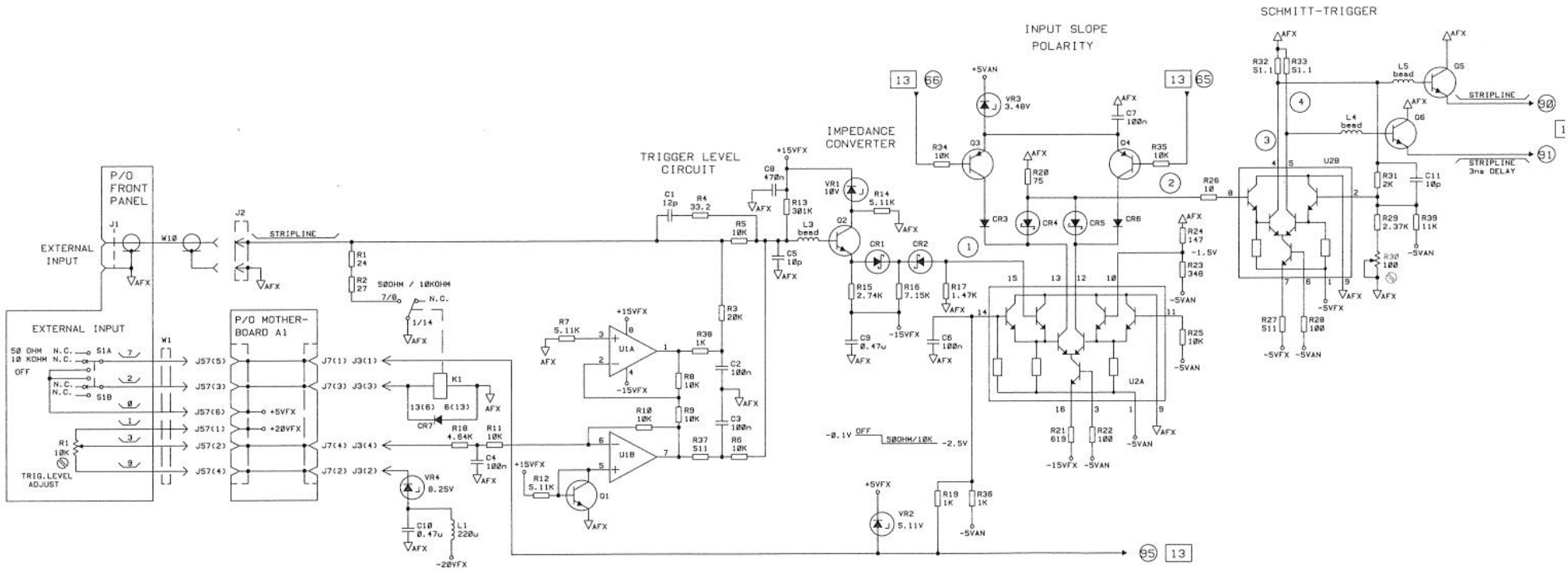
TABLE 6. PERIOD RANGES TRUTH TABLE

RANGE	SIGNAL "75"	SIGNAL "76"	SIGNAL "77"	SIGNAL "78"	SIGNAL "79"	SIGNALS "80/92"	SIGNAL "81"
1	1	1	-	1	1	1	1
2	1	1	-	1	1	1	1
3	First counter automatically enabled.-					-	-
4	1	1	1	1	0	0	0
5	1	1	1	0	0	0	0
6	1	1	0	0	0	0	0
7	1	0	0	0	0	0	0
8	0	0	0	0	0	0	0
TRIG	1	1	-	1	1	1	1

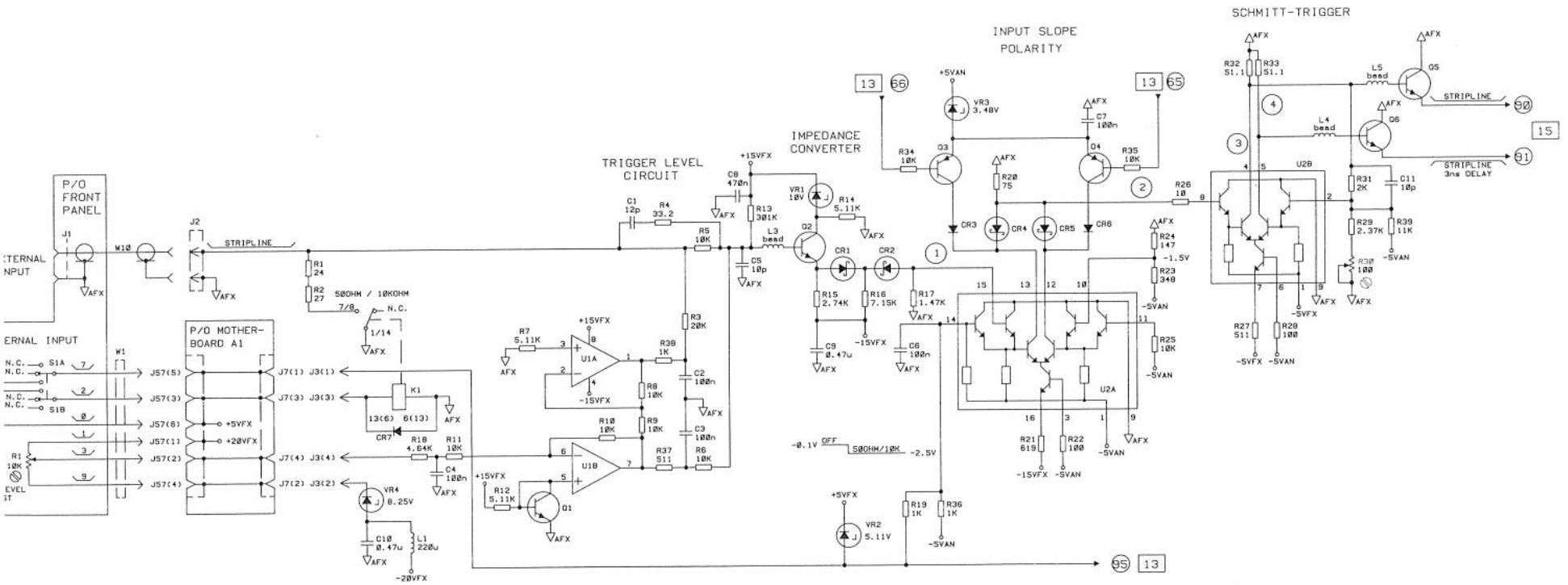

P/O A23 REP RATE GEN BOARD 08160-66523
TO MICROPROCE. BOARD A2 VIA J7 DEVICE BUS ON MOTHER BD A1
10 & 11
FOR DEVICE BUS DATA SEE DEVICE BUS TROUBLESHOOTING
VIA J6 POWER SUPPLY BUS ON MOTHER BOARD A1
6
FLOATING SUPPLIES
TO ANALOG CIRCUITS
TO DIGITAL CIRCUITS
NOTE: THESE VOLTAGES DERIVED FROM +5VFX AND -5VFX ON BOARD A18
INPUT MODE ACCEPTOR
LOAD
BIT1-BIT16
BIT1-BIT12
BIT7-BIT16
BIT9-BIT16
VCO CONTROL VOLTAGE
SLOPE (HIGH FREQ)
L SINGL
L VCO MA
14
95

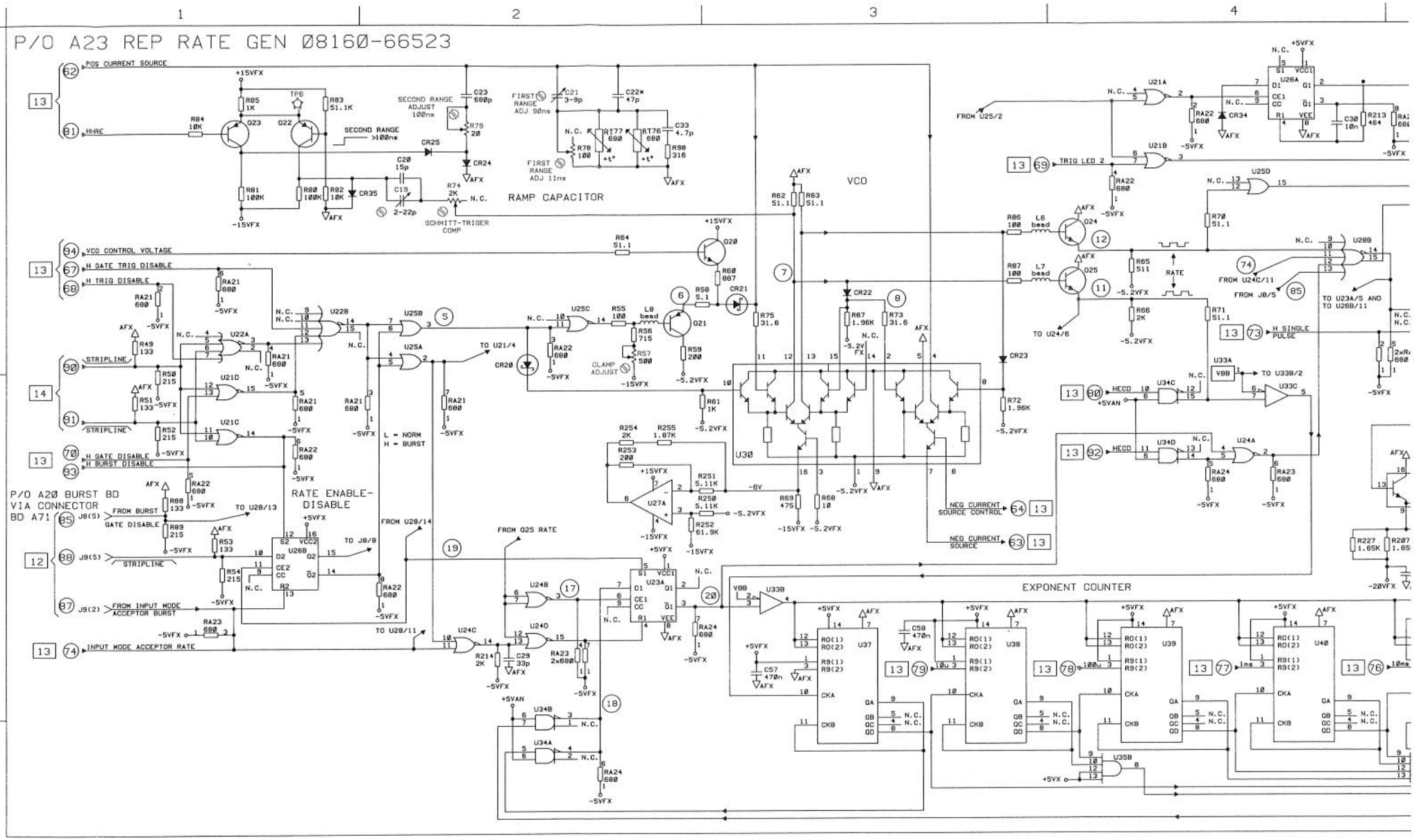

SERVICE
3
4
5
6
H SINGLE PULSE
HHRE
HECD
HECD
L VCO MAX
H TRIG DISABLE
H GATE DISABLE
L NEG SLOPE
L POS SLOPE
H GATE TRIG DISABLE
TRIG LED 2
H BURST DISABLE
VIA J7 ON
MOTHER BD A1 TO
BURST BD A2Ø
H BURST DISABLE
POS CURRENT SOURCE
NEG CURRENT SOURCE CONTROL
NEG CURRENT SOURCE
VCO CONTROL VOLTAGE
VCO CONTROL VOLTAGE
OFFSET (LOW FREQ)
SLOPE (HIGH FREQ)
BIT9-BIT16
7-BIT16
L SINGL
13
A23

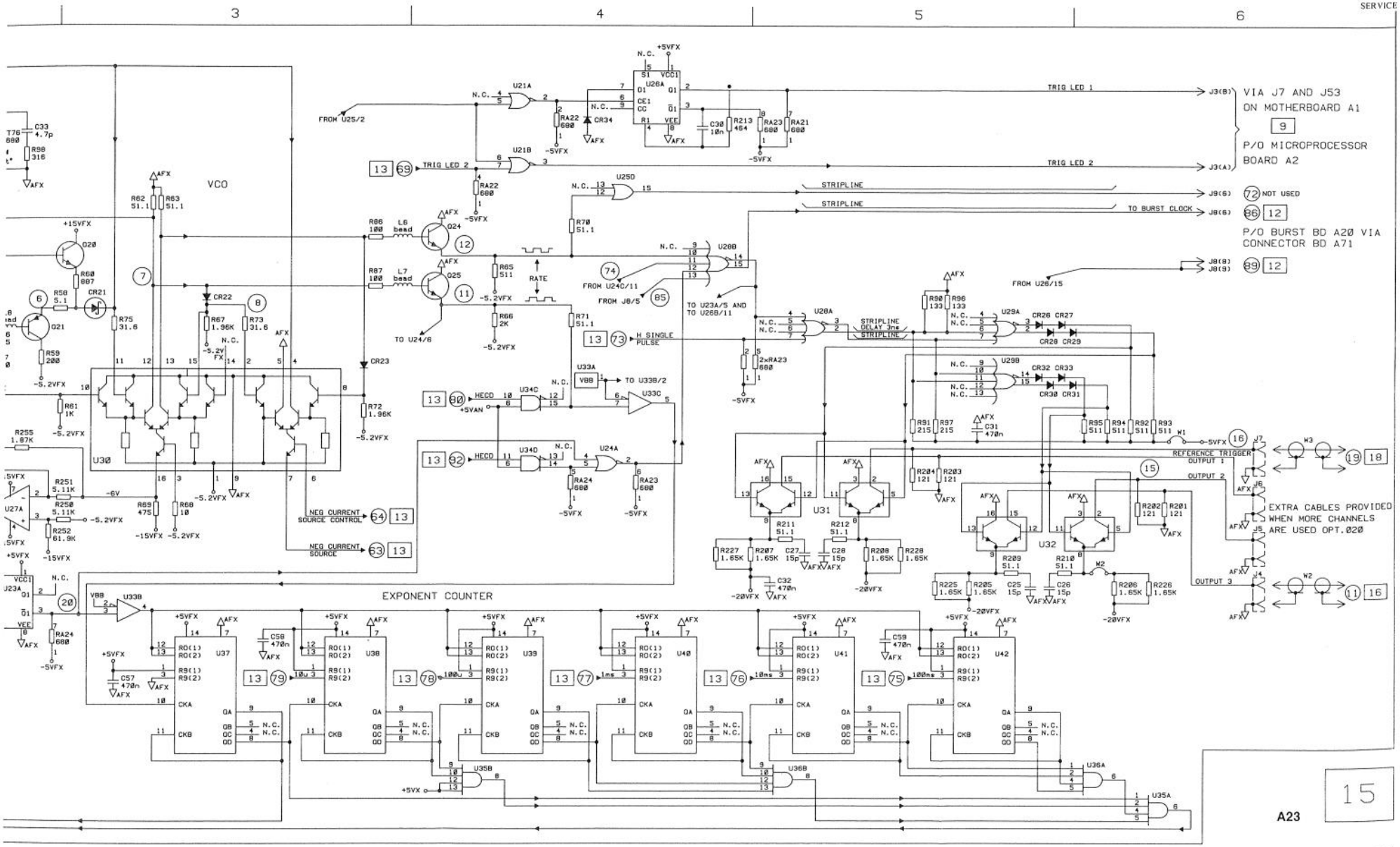
P/O A23 REPETITION RATE GENERATOR BOARD Ø8160-66523



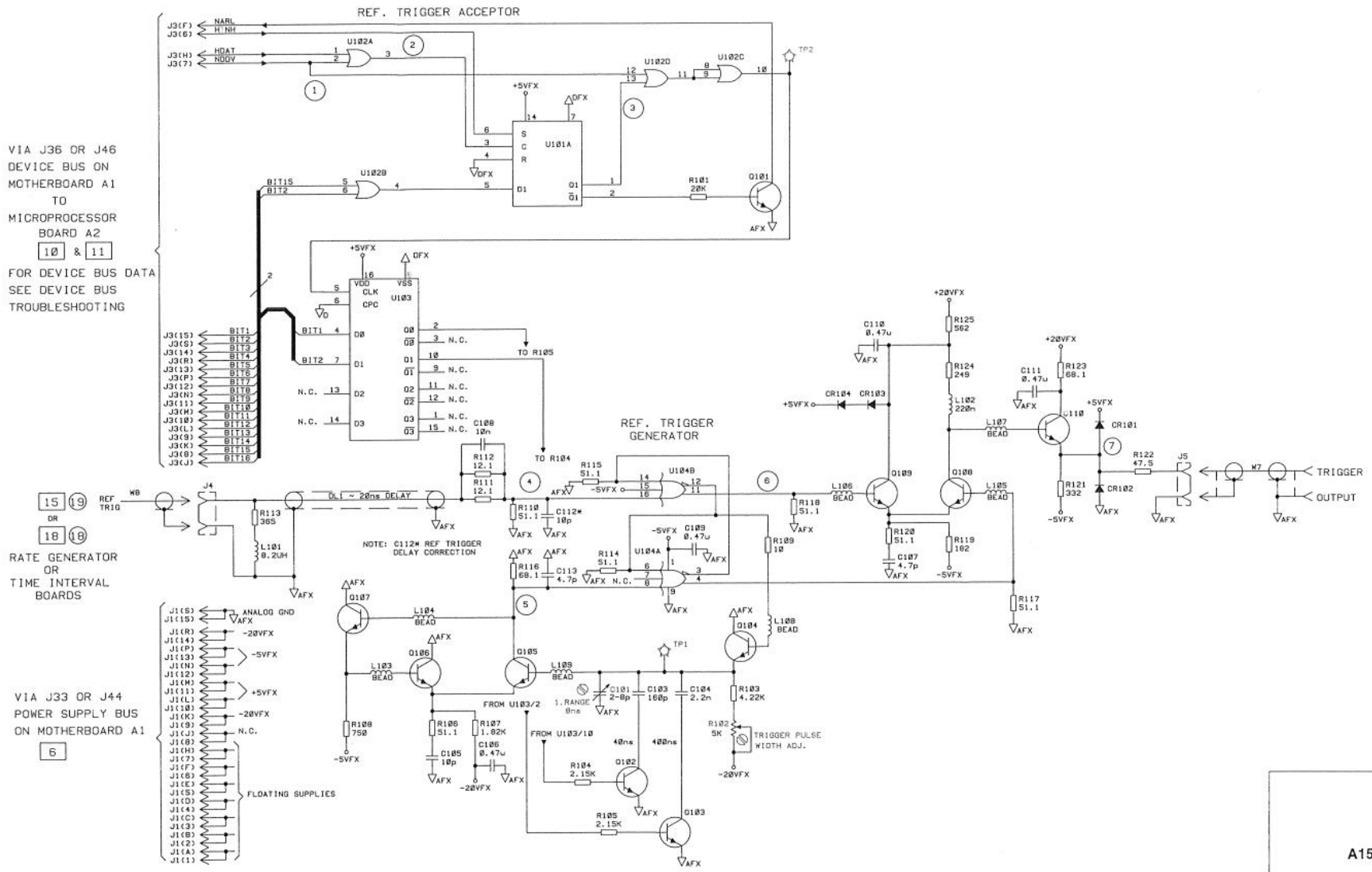
A23 REPETITION RATE GENERATOR BOARD Ø8160-66523




P/O A23 REP RATE GEN 08160-66523
POS CURRENT SOURCE
HHRE
SECOND RANGE ADJUST 100ns
SECOND RANGE >100ns
FIRST RANGE ADJ 90ns
FIRST RANGE ADJ 11ns
RAMP CAPACITOR
SCHMITT-TRIGER COMP
VCO
VCO CONTROL VOLTAGE
H GATE TRIG DISABLE
H TRIG DISABLE
STRIPLINE
H GATE DISABLE
H BURST DISABLE
L = NORM
H = BURST
P/O A20 BURST BD VIA CONNECTOR BD A71
FROM BURST GATE DISABLE
STRIPLINE
FROM INPUT MODE ACCEPTOR BURST
INPUT MODE ACCEPTOR RATE
RATE ENABLE-DISABLE
TO U20/13
TO U20/14
TO U20/11
TO J8/8
FROM Q25 RATE
TO U21/4
CLAMP ADJUST
NEG CURRENT SOURCE CONTROL
NEG CURRENT SOURCE
EXPONENT COUNTER
FROM U25/2
TRIG LED 2
RATE
FROM U24C/11
FROM J8/5
TO U23A/5 AND TO U26B/11
H SINGLE PULSE
TO U24/6
TO U33B/2
HECD
+15VFX
-15VFX
+5VFX
-5VFX
-5.2VFX
+5VAN
-6V
AFX
-5VFX
N.C.


3
4
5
6
VCO
EXPONENT COUNTER
TRIG LED 1
TRIG LED 2
STRIPLINE
TO BURST CLOCK
VIA J7 AND J53
ON MOTHERBOARD A1
9
P/O MICROPROCESSOR
BOARD A2
72 NOT USED
86 12
P/O BURST BD A20 VIA
CONNECTOR BD A71
89 12
FROM U25/2
FROM U24C/11
FROM J8/5
FROM U26/15
TO U23A/5 AND
TO U26B/11
TO U24/6
H SINGLE
PULSE
NEG CURRENT
SOURCE CONTROL
NEG CURRENT
SOURCE
REFERENCE TRIGGER
OUTPUT 1
OUTPUT 2
OUTPUT 3
EXTRA CABLES PROVIDED
WHEN MORE CHANNELS
ARE USED OPT.020
STRIPLINE
DELAY 3ns
STRIPLINE
U30
U31
U32
U37
U38
U39
U40
U41
U42
A23
15

P/O A15Ø OUTPUT AMPLIFIER CONTROL BOARD Ø8160-66550Ø



SB 8 REFERENCE TRIGGER

CONTENTS

ASSEMBLIES

A150, Output Amplifier
A23, Repetition Rate Generator

COMPONENT LAYOUT DIAGRAMS

See A150, Service Block 14
See A23, Service Block 7

SCHEMATIC DIAGRAMS

INTRODUCTION

The Reference Trigger signal is conditioned and output at the front panel as TRIG OUTPUT. It is the reference for the OUTPUT A/B pulse outputs.

The TRIG OUTPUT pulse width is 8ns, 40 ns, or 400 ns depending on the programmed repetition rate (PERIOD), except in the Triggered operating mode where is is always 8 ns.

The following table shows the programmed PER and corresponding TRIG OUTPUT pulse widths for the NORM, GATE, and BURST operating modes.

PER	TRIG OUTPUT	U103/Q0	U103/Q1
20 ns-99.9 ns	8 ns	0	0
100 ns-999 ns	40 ns	1	0
1 us-999 ms	400 ns	0	1

The Reference Trigger consists of the following circuits:

1. Control Flip-flop
2. Ramp Generator and Schmitt Trigger
3. Output Amplifier

REFERENCE TRIGGER ORIGIN

The Reference Trigger signal begins on the Repetition Rate Generator assembly A23. It is the buffered output of the VCO as is OUTPUT 1 and 2.

After being output from A23, the Reference Trigger signal goes to A127/U2 which is the Trigger Amplifier.

The Reference Trigger signal then goes to the Reference Trigger circuit on A150.

After conditioning by the Reference Trigger circuits on A150, the Reference Trigger signal is output as TRIG OUTPUT at the front panel TRIG OUTPUT BNC.

CONTROL FLIP-FLOP

The control flip-flop A150/U104 controls the output amplifier A150/Q108-110.

When the Reference Trigger signal sets A140/U104 at pin 16, the leading edge of the TRIG OUTPUT signal is generated by the output amplifier.

At the same time the control F/F U104 switches A150/Q104 off.

After the required time interval, the control F/F is reset by the Schmitt trigger which causes the output amplifier to switch and complete the TRIG OUTPUT signal.

RAMP GENERATOR

When the control F/F is reset by the Reference Trigger signal, the ramp switch A150/Q104 is switched off, and a negative ramp is generated at range capacitors A150/C101, C103, C104.

Range capacitors C103 and C104 are switched into the circuit by A150/Q102, Q103 which are controlled by the outputs of U103 which receives its data from the MPU.

When the ramp voltage reaches the trigger level of the Schmitt trigger, the Schmitt trigger switches and its pulse resets the control F/F at pin 8.

This causes the output amplifier to switch and complete the TRIG OUTPUT pulse.

OUTPUT AMPLIFIER AND SCHMITT TRIGGER

The output amplifier is controlled by the control F/F U104.

When a Reference Trigger signal sets U104, the leading edge of the TRIG OUTPUT pulse is generated.

When the control F/F is reset, the trailing edge of the TRIG OUTPUT signal is generated.